ATE

5800 Series Multi-functional, Multi-combinational Test System

The Aeroflex 5800 Series is designed to meet the ever-changing needs of today's fast evolving PCB manufacturing environment.

- Analog in-circuit and functional test
- Highly Configurable Test Platform (from PCB MDA to Unit functional test)
- Up to 3456 test points
- Integral PXI Capability
- Fast Program Development
- NET compliant software
- 3 body styles
- Configurable interface options
- Separate user and personality power supplies

Versatility

The 5800 Series is a multi-configuration multi-functional test system that is designed to meet the ever-changing needs of today's electronic manufacturing environment. An open approach to both hardware and software has been adopted. The open software architecture enables integration with code written using third party software such as Teststand™, Labview™, C# ™ and VB.NET™, in short any platform that is .NET compliant. The open hardware architecture allows configurable chassis and interface styles to accommodate low cost analog in-circuit testing, through to high integrity functional test solutions. The integrated 21-slot PXI based backplane enables the user to implement solutions using not only Aeroflex PXI cards but also cards from any PXI card supplier.

The 5800 Series of testers comprises three body styles. The 5860 is a floor-standing system that is ergonomically designed for high volume production. This compact system is particularly suited to in-line fixtured applications where its low height profile allows for SMEMA compliance.

The tester mass interconnect utilizes the industry leading commercially available Virginia Panel G12 interface * that provides a high density, compact and reliable connection between test system and test subject. This electro-mechanical interface can accommodate air, vacuum, power, digital and analog signals together with coax pins to ensure all test needs are supported.

The 5830 is rack mountable and facilitates easy cabling to an industry standard interface of the users choice, such as Everett Charles, MAC Panel or Virginia Panel. The 19 inch rack-mounted system is the easiest platform to integrate additional test resource that is not available in PXI format, such as GPIB controlled instrumentation, as it then can be contained within the one unit.

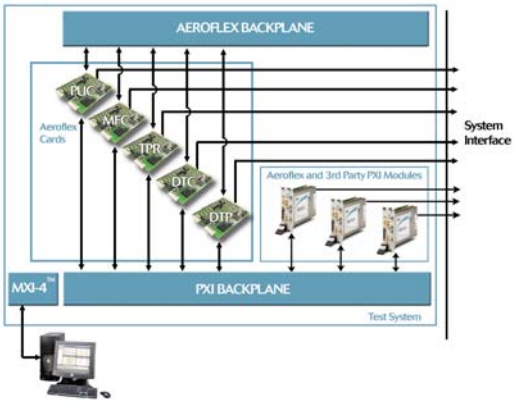
* - G12X also available

The 5820 benchtop model provides the same common core system but in a cost-effective package, making it an ideal solution for a test engineering department to facilitate development of applications away from the main production line. The Aeroflex and 3rd party PXI instrument cards are then interfaced to the test fixture by means of interconnecting cabling.

System Architecture

The Aeroflex 5800 Series is unique in the market place as it allows any 3U PXI instrument module to be used alongside the 5800's own test hardware. The system uses a National Instruments MXI-4™ card to seamlessly connect between the PC and the instrument cards, be they Aeroflex 5800 or 3U PXI cards from any vendor.

To give the system the ultimate flexibility and power, two backplanes have been incorporated into the design. The PXI backplane gives the 5800 the ability to benefit from the wealth of PXI cards available, whilst the Aeroflex backplane ensures that the integrity of fast in-circuit and functional signals between Aeroflex cards are maintained. Any 3rd party PXI or PCI card can be fitted to the 5800 and controlled by means of its OEM supplied driver software, which may be in the form of a DLL, Active-X control or .NET assembly. This allows the user to expand the functionality of the system without having to commission specially written software.



5800 Hardware

- ***Power and Utilities Card (PUC)*** - The PUC contains fixture utilities such as Fixture identification, control, sense, relays, power, actuation, UUT PSU isolation control, a data port and system health status.
- ***Test point relay card (TPR)*** - The test point relay card is the primary in-circuit interface to the unit under test (UUT). It routes from 4 global and 8 local analog busses to 192 testpoints via a matrix of fast switching relays (see TPR datasheet). In any 5800 system up to 18 test point relay cards can be fitted providing a maximum testpoint count of 3456 testpins per system.
- ***Multi-Function Card (MFC)*** - The MFC card provides the stimulus and measurement circuitry to enable analog in-circuit tests to be carried out in conjunction with a set of Test Point Relay cards, under the control of the 5800 Series controller.

  To enable these tests the card provides two reference generator channels, a current to voltage converter, two differential voltmeter channels, a guard amplifier, and a programmable resistor. The reference generator channels are referenced to system ground, but the differential voltmeter channels have a differential input, which can accept common mode voltages. This same hardware can also be used to perform analog functional testing.
- ***Digital Test Controller Card (DTC)*** - The DTC board plugs into the interface rack of the tester, and interfaces with both the PXI backplane and system backplane. The DTC contains a sequencer which controls execution of a digital test independent of the host PC. Configuration data and the test sequence are set up on the DTC card and the test is then started. From this point, the DTC controls the activity of the DTP cards via the system backplane until the test is complete. The DTC can also pause to allow other test activity (e.g. analog tests) to be performed or can trigger execution of analog tests while maintaining digital testpin activity.

  A single-step mode is available where runtime operation is paused at the end of each test step, but each instruction is executed at full speed using pin formats and timing. For very simple digital tests, the DTP testpoints can also be operated directly under software control.
- ***Digital Test Point Card (DTP)*** - The DTP has 64 non-multiplexed functional drive/sense channels that are relay-isolated to the fixture interface connectors. The board has analog access via a relay on each test point, thus allowing analog in-circuit tests to be performed in conjunction with an MFC card without the need to wire the same test point to a TPR card. The digital logic levels are programmable on a per board basis. Up to 18 digital test point cards can be used provide a maximum digital test point count of 1152.

Test point relay card (TPR)

Software Environment

Aeroflex's Integrated Development Environment (AIDE) is a powerful interactive environment that is simple to use allowing fast program development. It is a purpose built software environment that not only gives you access and control of the Aeroflex 5800 hardware but also gives you the tools to effectively utilise any 3U PXI hardware and other external instrumentation such as GPIB etc.

AIDE uses a mouse-driven "drag-and-drop" editing system for fast and accurate program development that ensures developed code is syntactically correct. All the components of the user interface act as a cohesive unit, which presents the developer with the complete state of both the program and the hardware. This allows the user to make fully informed decisions during program development.

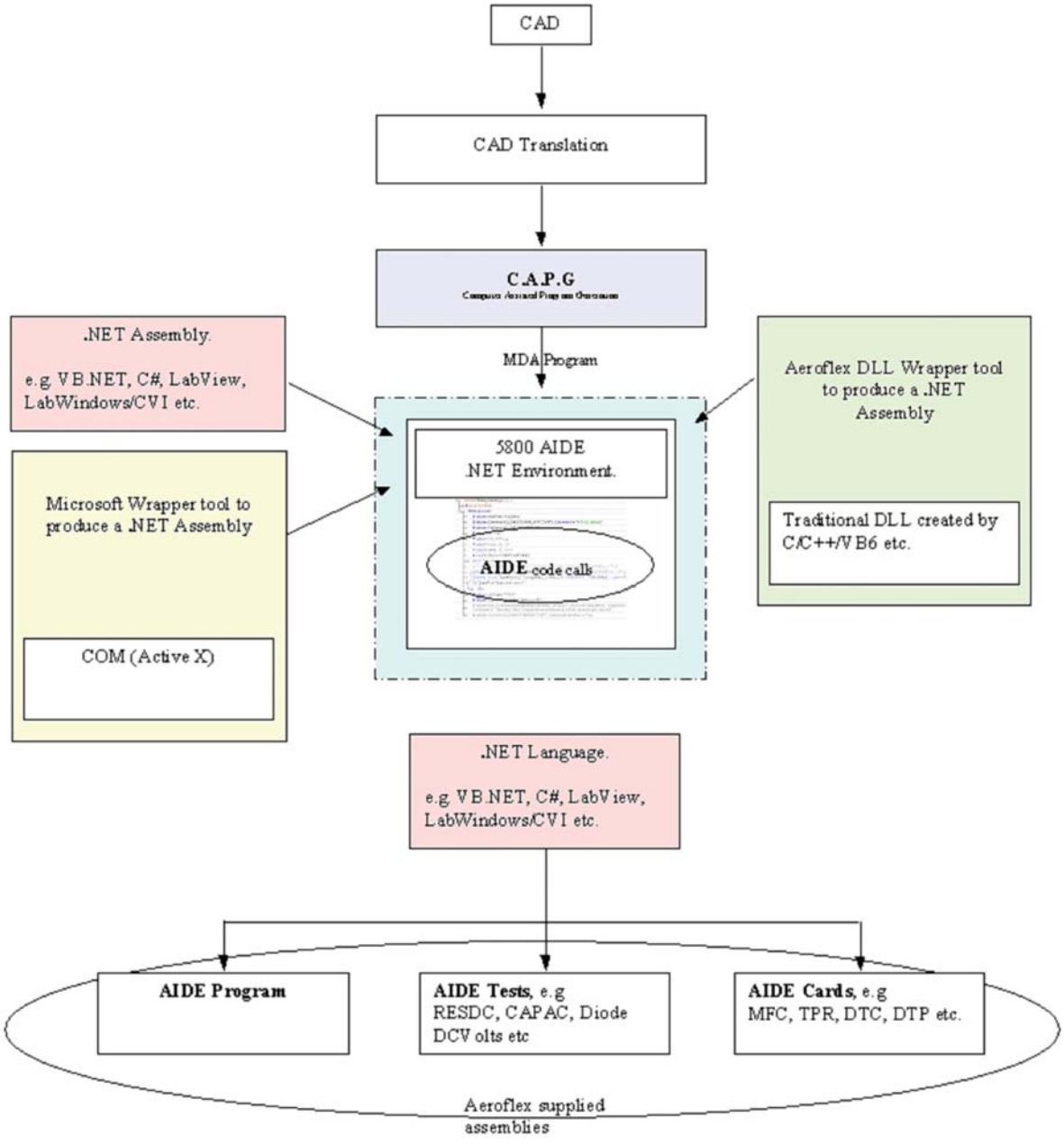
AIDE gives the user a full set of debug tools which provides the ability to modify code and variable values during the debug and execution of the program. This can dramatically shorten development times, as there is no need to terminate a program to make edits and then re-execute.

AIDE is based on the .NET platform, and allows the AIDE programmer access to the entire .NET Framework. This provides a class library that allows the user to save many hours of program development by using the functionality that it contains.

Software Integration

The open approach that has been adopted by the Aeroflex software enables integration with code written using third party software that is .NET compliant, such as Teststand™, Labview™,C#™, VB.NET™.

- Any .NET programming environment can be used to access and control the 5800 Series hardware.
- AIDE can use code developed in any .NET environment, enabling code developed during the test and development stage of a new product to be re-used in production test.
- Any resource with DLL, .NET or Active X drivers can be controlled by AIDE.
- Test programs developed in AIDE can be executed from any .NET aware software environment.



ANALOG AND DIGITAL TESTING

The 5800 Series builds on the Aeroflex reputation of supplying the fastest test systems on the market. Analog test speed is the area where the largest gains can be made in improving overall test time and this is achieved by the use of the following techniques:

- Device pre-charge facility
- Custom fast switching relays

Due to the high level structure of the AIDE environment, the writing and modifying of analog tests is simple. All analog tests use a common format to describe the appropriate test parameters. The purpose of these tests is to implement what can be complex test methods within a very simple statement. The graphical commissioning tools, supplied as standard, further simplify the process by guiding the user, through use of dropdown menus to ensure the correctly formatted instructions, thus eliminating syntactical errors.

The digital functional sub-system comprises a DTC card, together with up to 18 DTP cards. A digital test consists of parallel sets of drive and sense patterns applied to the test subject to verify correct operation under control of the DTC microprogram sequencer.

Pattern generators allow the test engineer to program address data into a block of memory, which can then be used in conjunction with the CRC hardware in order to carry out Signature Analysis (Cyclic Redundancy Checks) on devices.

When programming a device the pattern generators are loaded with the data to be programmed. This data could be within the test program, or stored on a disk. The method chosen depends on the volume of data to be programmed, generally the larger the data the more inclined it is to be stored on disk. The pattern generators then download the data to the device under test. All of this procedure is executed using AIDE therefore powerful operations are executed with simple instructions.

The DTC supplies 64 bits of pattern generator data along the system backplane for use on the DTP cards to control the activity on selected testpins. The 64 bits are sourced from a set of 4 16-bit pattern generators. Each pattern generator consists of a block of RAM, addressed by a configurable counter. The counters have programmable count lengths, and may be cascaded together to generate wider/longer counts. The RAM is loaded with the required test pattern before the start of a test run.

Parallel outputs from the generator may optionally be converted into serial data and transmitted along the backplane lines, which may similarly be used as a source of DTP instruction data.

Every testpin of the digital sub-system has the ability to switch between a digital and analog resource, this is a key feature when testing mixed signal devices such as ADCs, DACs etc. Every testpin is provided with terminator circuitry to enable testing of tristate buses and open collector devices. The skew for both drive and sense channels of any given testpoint is carefully controlled to ensure the test vectors delivered to the tester interface are of the highest integrity.

The DTC has an internal clock speed of 200 MHz, allowing vector rates of 10 MHz with 5 ns edge placement, this specification allows comprehensive testing of the most complex and demanding devices today. The 5800 digital test system also includes a range of advanced features, such as internal PXI triggers, pin formatting and variable timing sets. On-the-fly jumps allow program flow decisions to be made at full speed within an individual digital test.

TEST PROGRAM GENERATION

To produce a test program and fixture the fundamental requirement is information on the product to be tested. The type of information required is related to the electrical characteristics of the product (e.g. value of components fitted) and the mechanical characteristics (to enable the fixture to be manufactured). This information can be entered manually, or from CAD data.

The preferred method is to obtain the information from CAD data. The reasons for this are that it is quicker to read in a data file than typing in all the information, and there is less chance of error being introduced to the process. There are many CAD formats available and as such the recommended Aeroflex solution is to use either eM-Test Expert or CAMCAD to produce a .CB file (Aeroflex circuit board description file) that can then be imported into the program generation software (CAPG). This approach ensures that time-to-market is maintained by the generation of quick and accurate fixture and program data.

CAPG

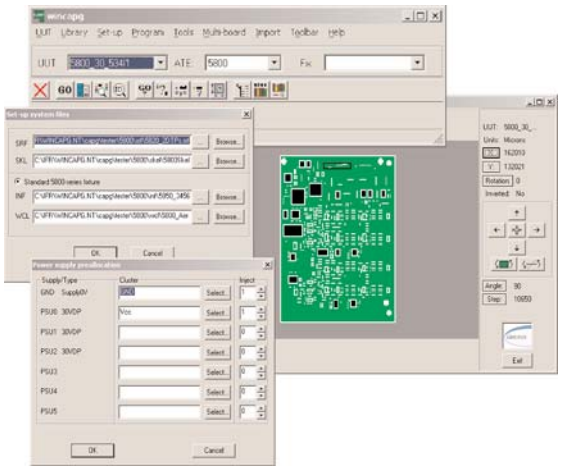
The menu driven Aeroflex Computer Assisted Program Generation (CAPG) software enables the test engineer to automatically generate test program and fixture information for analog in-circuit tests. The software can be run on a PC running a 32 bit Microsoft Windows operating systems (i.e. Windows XP or 2000). The software is provided with a site license allowing any number of off-line programming stations.

When generating the test program and fixture information the test engineer follows a number of defined and logical steps. Briefly those steps are:

- Import the circuit board description file.
- Include/define tests libraries for new devices.
- Generate tests for devices.
- Generate test program and fixture information.

At each stage warnings and errors are generated so that the test engineer can modify data to suit their needs as appropriate.

If the test engineer decides that they wish to deviate from the standard device libraries the flexible design approach of CAPG allows them to do so. The test engineer can set up their own libraries where the modified device models are held.



Test Generation

Having imported the .CB file, CAPG will analyze the circuit description and generate the necessary device tests, together with guard points where appropriate. A SPICE circuit simulation tool will then verify the predicted performance of these tests by simulating the test conditions applied to a given component. Any deviations from the expected measurement result will be reported for use when commissioning the test program.

Multi-Board

When testing products that are manufactured as a number of individual boards within a pallet, problems can arise with the use of a program that tests the boards as one. This potential problem is due to the fact that each board in the pallet could have different test and tolerances applied during the debug process. The concept of separate code could lead into quality issues due to the same product being tested to different standards. Therefore the ideal scenario is to have one set of test code to test all boards.

This is achieved on the 5800 Series using the Multi-Board software within CAPG. When this software is used a set of test code is produced that produces a master control program which calls up the test code using appropriate testpins for each board. The advantage of this is that one set of test code is used to test all the products contained on a given pallet, hence reducing potential quality issues.

Fixturing

Once the test program has been generated the next stage is to produce the necessary information for fixture manufacturing. As well as the basic build style of the test fixture, fixture manufacturers need to know x-y positions of the test pins and where they are wired. How this information is produced can depend on the fixture manufacturer. Some manufacturers will take the standard files produced by CAPG and process it themselves into the format required by their machines and people. Other fixture manufacturers prefer to receive the data already formatted. If the requirement is the latter then using the 'Fixture Build Output' utility within CAPG allows the test engineer to define the output format of the wiring files.

TEST PROGRAM COMMISSIONING

Test programs require modification for one of three reasons:

- Engineering change
- Fixture modification
- Commissioning a new program and fixture

Traditionally the tasks of modifying test programs have required the skills of a test engineer who has in-depth knowledge of both testing and the tester. The effect of this is that changes and modifications could only be carried out successfully by the appropriate test engineer, hence extending the time it takes to implement a change.

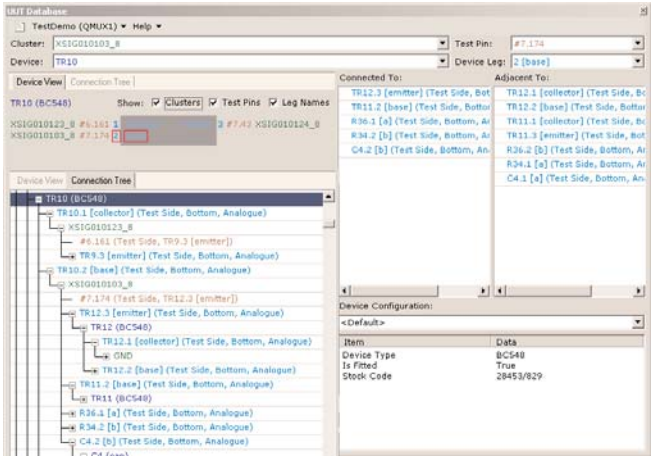
To ensure that the effects of changes are minimized, and can be carried out by anyone with the appropriate authority, the 5800 provides a suite of commissioning tools. The use of these tools produces a number of benefits:

- Reduces the need to consult manuals or on-line help since the syntax is already provided
- Ensures that you have instant feedback, e.g. using the test stability tool assists in reducing the cases of no fault founds on the production line
- Reduces the time it takes to implement changes
- Ensures that the machine is easy to use

These tools provide the test engineer, whether they are experienced or not, with easy to use graphical tools which ensure quality test programs are produced easily and cost effectively.

Graphical Database Display

The 5800 database file is interrogated at runtime by the test program to provide additional failure information when a manufacturing fault occurs. It also provides valuable information for both analog and functional commissioning via the database display.



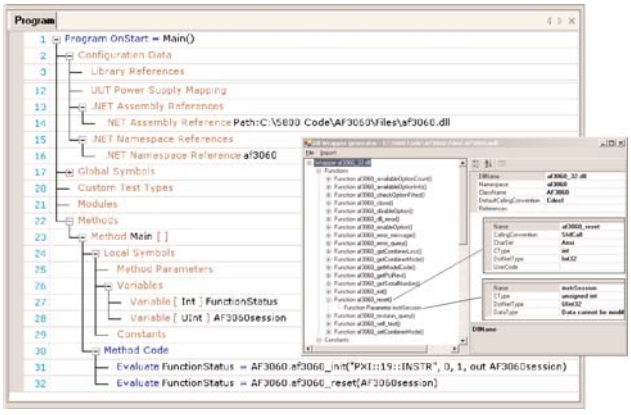
Statistical Display Tool

If a test has not been correctly debugged it can lead to unstable measurements being made. The effect of this is that the 5800 will report a false fail on the component in question. To aid the test engineer in assessing the stability of passive component tests the 5800 Series comes with the Statistical Display Tool.

FUNCTIONAL TESTING

The open approach that has been adopted by Aeroflex for the test environment allows the use of any third party software that is .NET compliant. This means that software and hardware integration of PCI or PXI instrumentation has never been easier. The AIDE software allows the user to simply import the .NET assembly for any given instrument and use it as if it were running under any of the industry standard test languages. The flexibility of AIDE also allows import of Active X controls and DLLs via the supplied DLL Wrapper Tool.

DLL Wrapper Tool



The DLL wrapper tool allows a wrapper to be generated for any traditional DLL. A primary use of this is for use with PXI cards where .NET assemblies or Active X controls are not supplied or available. The DLL wrapper tool can import the "C-Header" file for the DLL, which is supplied by the DLL supplier. The functions, type definitions and constants defined in the header file are then all seamlessly available in an AIDE test program.

ADVANCED TEST TECHNIQUES

Boundary Scan

The 5800 Series Digital Functional sub-system fully supports the IEEE1149.4 boundary scan standard and integrates with both JTAG Technologies and Goepel platforms. Integration is achieved through the use of the supplied controller card (PXI, PCI etc.) and associated interconnects, thus allowing boundary scan test programs to be executed under the control of the AIDE environment. The advantage of this is that programs that have been developed for the debugging of new designs or for bench testing of prototypes can now be re-used in production test.

During the execution of the boundary scan program, the DTP can be added to the boundary scan chain and used to provide external stimulus to the UUT in order to effect the behavor of peripheral components (disable or configure device etc.). AIDE handles the resultant fault reporting transparently, giving a totally integrated run time solution.

In-system Programming (ISP)

The 5800 Series test system can extend to ISP programming through the AIDE integrated environment, thus allowing device programming and verification as part of the board test cycle.

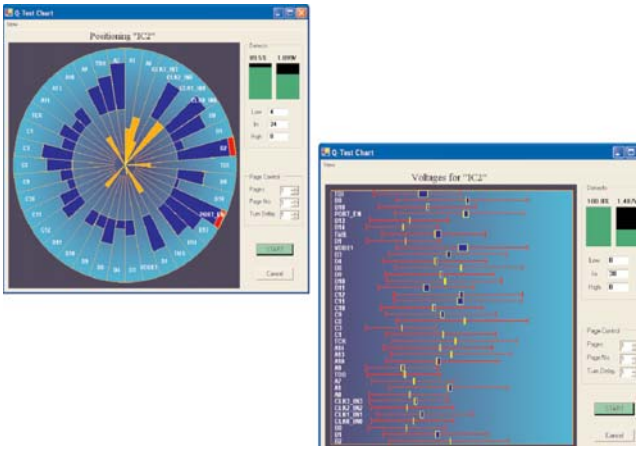
By using the 5800 to perform both JamTM (STAPL) and Serial Vector File (SVF) device programming, it eliminates the need for stand-alone device stations. This provides a great saving in terms of both time and money.

Vectorless Test

The standard way of testing integrated circuits is known as vector testing. This is where signals are supplied to the device under test, and the response to those signals is measured. These test vectors are usually taken from the appropriate library model for the device. However today's designers are now using more and more application specific devices, for which there may not be library models.

Aeroflex was the first to provide a solution to this issue with the patented Q-Test. This technique verifies that the legs of the device under test have been correctly soldered, with only the device pin list data provided. No matter how large or complex a device is a test can be generated in a fraction of the time it takes to provide a conventional vector test.

The 5800 Series utilizes the latest developments in vectorless test, through the use of capacitive probes and fixture mounted circuitry. This technique enhances any digital functional application by ensuring components legs on any given device are correctly soldered to the board prior to the functional routine being executed.



SPECIFICATION

GENERAL TEST CAPABILITIES

Full analog in-circuit test

Digital functional test

Functional Test (using 5800 instrument cards and/or PXI cards)

Advanced Test Techniques

IEEE 1149.1 Boundary Scan (JTAG/Goepel)

Vectorless test

GPIB

Device Programming

Computer System (minimum)

2.8 GHz Pentium™ 4 based PC with 1 Gbyte of RAM

2 spare PCI slots

4 USB ports

CD ROM

17" Flat Panel Monitor

Operating System

Windows 7 (32 bit) Professional

Testpoint Count

192 - 3456 analog non-multiplexed test points

64 - 1152 analog/digital non-multiplexed test points

ANALOG TEST FACILITIES

CONTACT TEST

Less than 100 KΩ or Diode in series with 20 KΩ

900 pins per sec

Link and Track

Range

1 Ω to 100 Ω

Accuracy

±10%

Track Speed

Up to 6000 pins per second depending on circuitry

Link Speed

Up to 350 links a sec

RESISTANCE DC

Normal Mode

Range

100 Ω to 10 MΩ

Accuracy

100 Ω to 100 KΩ: ±1% ±0.1 Ω

>100 KΩ: ±1.5%

Speed

Up to 1000 per second, dependent on resistor value

Guarding Ratio

1000:1

Low Impedance Mode

Range

1 Ω to 1 KΩ

Accuracy

±0.7% ±10 mΩ

Speed

Up to 700 tests per second, dependent on resistor value

RESISTANCE AC

Normal Mode

Range

100 Ω to 100 KΩ

Test Frequency

100 Hz, 1 kHz, 10 kHz

Accuracy

±3% ±1 Ω

Test Speed

Up to 700 tests per second, dependent on resistor value

Low Impedance Mode

Range

1 Ω to 100 Ω

Test Frequency

100 Hz, 1 kHz, 10 kHz

Accuracy

±3% ±0.1 Ω

Test Speed

Up to 700 tests per second, dependent on resistor value

CAPACITANCE AC

Normal Mode

Range

0 pF to 1 uF

Test Frequency

100 Hz, 1 kHz, 10 kHz

Test Voltage

200 mV peak or user selectable

Accuracy

±3% ±4 pF

Test Speed

Up to 700 tests per second, dependent on capacitor value

Low Impedance Mode

Range

1 uF to 10 mF

Test Frequency

100 Hz, 1 kHz, 10 kHz

Test Voltage

200 mV peak or user selectable

Accuracy

±3% ±4 pF

Test Speed

Up to 700 tests per second, dependent on capacitor value

CAPACITANCE DC

Range

≥10 uF

Accuracy

±3%

Test Speed

Up to 100 tests per second dependent on capacitance value and charging current

INDUCTANCE

Normal Mode

Range

1 mH to 100 H

Test Frequency

100 Hz, 1 kHz, 10 kHz

Accuracy

±5% for Q>15

Test Speed

Up to 400 tests per second dependent on inductance value

Low Impedance Mode

Range

1 uH to 10 mH

Test Frequency

100 Hz, 1 kHz, 10 kHz

Accuracy

±3% ±0.2 uH for Q>15

Test Speed

Up to 400 tests per second dependent on inductance value

DIODE/LED

Diode On Test

Diode OFF Test

Diode Leakage Test

Up to 750 tests per second

Zener Test

Zener On test

Zener OFF Test

Zener Leakage Test

Up to 750 tests per second

Transistor Test

Transistor On Test

Transistor Off Test

Transistor HFE Test

Up to 750 tests per second

FET Test

FET On Test

FET Off Test

FET RDS Test

Up to 750 tests per second

Transformer Test

Performs an AC ratio test

Up to 650 tests per second

GENERAL PURPOSE ANALOG FACILITIES

REFERENCE GENERATOR CHANNELS (2 off)

Voltage Range

-10 V to +10 V DC

Low range: 0.01 to 1 V AC peak

High range: 1 to 10 V AC peak

Resolution

16-bit normal

12-bit DDS

Accuracy (DC)

±1% ±5 mV

AC Accuracy (Standard frequencies)

High range:

±1% ±10 mV

Low range:

±1% ±1 mV

Frequency (sine wave)

0.1 Hz to 50 kHz normal

1 Hz to 200 kHz DDS

AC Distortion

Typically better than 0.2%

Settling Time

Typically less than 50 usec

Current Ranges

10 to 250 mA (high range)

0.1 to 10 mA (low range)

Resolution

14-bit

Accuracy (DC)

100 uA to 10 mA: ±1% ±15 uA

>10 mA to 250 mA: ±1% ±0.3 mA

PROGRAMMABLE RESISTOR

1 Ω - 100 Ω ±2.5%, in decade steps

1 KΩ - 10 MΩ ±1.5%, in decade steps

VOLTAGE MEASUREMENT CHANNELS (2 off)

Range

±100 mV to ±100 V full scale peak in 7 ranges

Input Protection

±100 V

DC Accuracy

Range	*without Filter*	*with Filter*
100 V	*±0.5% of reading ±100 mV*	*±0.6% of reading ±200 mV*
25 V	*±0.5% of reading ±25 mV*	*±0.6% of reading ±50 mV*
10 V	*±0.4% of reading ±10 mV*	*±0.5% of reading ±20 mV*
2.5 V	*±0.4% of reading ±2.5 mV*	*±0.5% of reading ±5 mV*
1 V	*±0.5% of reading ±1 mV*	*±0.6% of reading ±2 mV*
0.25 V	*±0.5% of reading ±0.5 mV*	*±0.6% of reading ±1 mV*
100 mV	*±0.5% of reading ±0.2 mV*	*±0.6% of reading ±0.4 mV*

AC Accuracy

Range	*without Filter*	*with Filter*
100 V	*±2% of reading ±200 mV*	*±4% of reading ±400 mV*
25 V	*±2% of reading ±50 mV*	*±4% of reading ±100 mV*
10 V	*±2% of reading ±20 mV*	*±4% of reading ±40 mV*
2.5 V	*±2% of reading ±5 mV*	*±4% of reading ±10 mV*
1 V	*±2% of reading ±2 mV*	*±4% of reading ±4 mV*
0.25 V	*±2% of reading ±0.5 mV*	*±4% of reading ±1 mV*
100 mV	*±2% of reading ±0.2 mV*	*±4% of reading ±0.4 mV*

Resolution

16-bit

Bandwidth

200 kHz, approximately

Test Speed

Up to 700 tests per second

Noise Filter

8 pole elliptic, programmable cut-off frequency between 10 kHz and 150 kHz in steps of 10 kHz

Anti-alias Filter

Switchable between linear amplitude (3-pole Butterworth) and linear phase

Input Resistance

100 V and 25 V Ranges

Nominally 10 MΩ to ground at each terminal / 20 MΩ differential

Other Ranges

Nominally 1 MΩ to ground at each terminal /

2 MΩ differential or >100 MΩ selectable

CURRENT MEASUREMENT

Current Ranges

0 to ±2.5 uA, up to ±250 mA in 6 ranges

DC Accuracy

±2% of reading ±0.1% full scale

Bandwidth

DC to 100 kHz depending on Frequency

Measurement Speed

Up to 700 tests per second

TESTPOINT RELAY CARD (TPR)

Maximum Input Voltage

100 V DC or 100 V AC peak maximum differential between any two points or relative to system ground

Current Capability

500 mA maximum carry or switched

Switch Power

10Ω maximum

Pin-Pin Capacitance

5 pF maximum to an adjacent test point excluding fixture wiring

Capacitance to Ground

50 pF relay open

400 pF single relay to internal bus closed

Series Resistance

500 m max, backplane analog bus connector to fixture interface

Isolation

>1 x $10^{11}\Omega$

GUARD AMPLIFIER

Offset Voltage

±2 mV

Bias Current

±10 nA

Output Current

250 mA max @ ±10 V

Input Voltage Range

±10 V max

DIGITAL TESTING

GENERAL CAPABILITY

Microprogram Sequencer Memory Depth

64 k test steps, each test step consists of a programmable number of sub-steps from 4-512

Microprogram Control Instructions

Instruction set includes: jump, loop, subroutine call/return, repeat, delay, conditional operations, pause, stop. Single step operation available.

Test Step Period

100 ns min (10 MHz test step rate), with increments of 5 ns, or synchronized to external clock from the UUT.

Edge Placement Resolution

5 ns min

Sub-Step Length

Sub-step length is a programmable number of master clock periods. Each master clock period is 5 ns (internal clock), or dependent on an external clock routed via PLL clock generator which provides programmable multiply and divide ratios.

Sub-Step Timing

There are 16 sets of user-programmable waveforms that may be applied to 8 physical timing lines. Each set of waveforms is known as a timing set. Timing sets are selectable at runtime, from microprogram instruction. Each physical line is selectable for use as drive or sense, but not both, for a particular test run. Minimum pulse width per timing line is 20 ns.

Data Compression

16-bit indirect vector address applied to DTP cards.

Pattern Generators

4 software-loadable pattern generators on DTC (global resource), each with 1 M x 16 RAM. Pattern generators have variable count length, and may be linked to generate up to 64 bit-wide pattern. Pattern generator data may also be serialized (16:1 or 64:1) and transmitted along 4 GPIO lines for use by the DTP, giving up to 64M-bit long pattern without reload.

Trace Ram

For tracing program flow. 256 k locations, compressed

Triggers

Access to the PXI trigger bus is provided

Internal Master Clock

Accuracy

200 MHz + 0.1%

External Clock

The external clock input may be either direct, or via a clock generator with programmable multiply/divide ratios to generate a higher or lower frequency than the external clock. The resultant clock, either direct or via the clock generator is multiplied by 4 to generate the master clock.

Number of Input Channels

4

Input Frequency Range (direct or via clock generator)

1 MHz - 50 MHz

Input Type

LVTTL input, 100 R series resistor and 10 kR pullup to +3.3 V.

Input Voltage Range

0 - 5.5 V

Termination

50Ω || 10 pF or none, relay selectable

Polarity

Selectable high or low

Delay

8-bit programmable, 0.5 ns per bit

External Sync A/B Inputs

Two sync input circuits (A/B) are provided. When programmed for external sync, runtime activity is held until the programmed sync input is set active from the UUT.

Number of Input Channels

4

Input Type

LVTTL input, 100 R series resistor and 10 kR pullup to +3.3 V.

Input Voltage Range

0 - 5.5 V

Termination

50Ω || 10 pF or none, relay selectable

Polarity Selectable high or low

Triggering

Level sensitive

External Event Input

An input to the condition logic that may be used to control conditional program flow.

Number of Input Channels

4

Input Type

LVTTL input, 100 R series resistor and 10 kR pullup to +3.3 V.

Input Voltage Range

0 - 5.5 V

Termination

50Ω || 10 pF or none, relay selectable

Triggering

Level sensitive

DIGITAL TESTPOINT CARD (DTP)

GENERAL CAPABILITY

Analog Routing

Connect to a single or multiple internal busses with 1 relay per testpoint, with a matrix to the global analog bus

Immediate Mode

Immediate mode operation is available, where drive and sense operations can be programmed independent of the DTC microprogram controller

Boundary Scan

A boundary scan mode is available, where the testpoints may be included in a boundary scan path on the UUT

Fixture I/O FPDx

A set of digital inputs to the testpoint control FPGAs, may be used as a source of pattern data, or as part of the boundary scan port when the board is used in boundary scan mode. LVCMOS level inputs, with 470R series resistors and pull-up/down resistors:

FPD0, FPD2

10 kΩ to GND

FPD1, FPD3

10 kΩ to 3.3 V

Fixture Boundary Scan TDO

FTDO signal, used when the board is in boundary scan mode. LVCMOS output

Fixture Grounds

Both switched and fixed grounds are available at the interface connectors

Digital Testpoint Characteristics

Testpoint Instruction Memory

16 k x 4 bits per testpoint, addressed at runtime by the DTC microprogram vector address. Each instruction memory location contains an index to the testpoint instruction arrays, which are 64-bits wide per-testpoint. This allows complex and variable instruction sets to be created

Testpoint Learn Memory

16 k x 4 bits per testpoint

Testpoint Skew

+10 ns maximum skew between any 2 testpoints, driving or monitoring, when programmed to the same drive voltage level and drive strength and under no-load conditions. Skew specification applies at the interface connectors, and does not include additional effects of cables

Maximum Input Voltage

+100 V logic relay open

Drive High Voltage logic relay closed

Stray Capacitance

150 pF maximum, to GND, driver off, logic relay closed

50 pF maximum to GND, logic relay open

5 pF maximum to adjacent testpoint, logic relay open

400 pF maximum to GND, relay to internal analog bus closed

Leakage Current into Analog Bus Lines

20 nA maximum per analog bus line

Resistance to GND

100 MΩ to GND, logic relay open

Relay Switch Current

500 mA, 10Ω switching power maximum

Relay Carry Current

500 mA maximum

Testpoint Driver Specification

Driver Vcc Range

2 V to 5.1 V

Driver Vcc Resolution

15 mV

Formats per Testpoint

Non-return to Zero (NRZ)

Return to Zero (RZ)

Return to 1 (R1)

Return to Inhibit (RI)

Return to Complement (RC)

Delayed Non-Return to Zero (DNRZ)

Drive Strength

4 selectable drive strengths, 500, 140, 80, 60 nominal output impedance

Driver Level Accuracy

+3.7% +75 mV

MAXIMUM DRIVE LOW VOLTAGE

Drive High Voltage = 3.0 V

0.5 V

5.5 mA load, 50 Ω output impedance

17 mA load, 14 Ω output impedance

27 mA load, 8 Ω output impedance

37 mA load, 6 Ω output impedance

Drive High Voltage = 4.5 V

0.5 V

7.5 mA load, 50 Ω output impedance

29 mA load, 14 Ω output impedance

48 mA load, 8 Ω output impedance

65 mA load, 6 Ω output impedance

MINIMUM DRIVE HIGH VOLTAGE

Drive High Voltage= 3.0 V

2.7 V

50 uA load, all drive strengths

2.26 V

6 mA load, 50 Ω output impedance

17 mA load, 14 Ω output impedance

28 mA load, 8 Ω output impedance

38 mA load, 6 Ω output impedance

Drive High Voltage = 4.5 V

4.2 V

50 uA load, all drive strengths

3.56 V

11 mA load, 50 Ω output impedance

33 mA load, 14 Ω output impedance

54 mA load, 8 Ω output impedance

73 mA load, 6 Ω output impedance

DRIVER OUTPUT CURRENT

Continuous

25 mA, 50 Ω output impedance

50 mA, 14 Ω output impedance

75 mA, 8 Ω output impedance

100 mA, 6 Ω output impedance

Dynamic

30 mA, 50 Ω output impedance

100 mA, 14 Ω output impedance

175 mA, 8 Ω output impedance

250 mA, 6 Ω output impedance

Driver Output Impedance (Nominal 6R)

Accuracy	***2.0 V***	***3.3 V***	***5.0 V***
	8.5 Ω +5.0 Ω	*5 Ω +3.5 Ω*	*3.5 Ω +2.9 Ω*

Driver Output Impedance (Nominal 8R)

Accuracy	***2.0 V***	***3.3 V***	***5.0 V***
	11.5 Ω +7.2 Ω	*7 Ω +4.3 Ω*	*5 Ω +3.5 Ω*

Driver Output Impedance (Nominal 14 R)

Accuracy	***2.0 V***	***3.3 V***	***5.0 V***
	20 Ω +9.1 Ω	*12 Ω +6.1 Ω*	*9 Ω +5 Ω*

Driver Output Impedance (Nominal 50R)

Accuracy	***2.0 V***	***3.3 V***	***5.0 V***
	65 Ω +21 Ω	*50 Ω +13 Ω*	*45 Ω +12 Ω*

TESTPOINT MONITOR SPECIFICATION

Voltage Range

0 V to +5.1 V

Accuracy

+ 3.9% + 65 mV

Reference Setting Resolution

20 mV

Input Impedance

20 KΩ + 10% terminators off

Testpoint Terminator Specification

High and low impedance terminator resistors, selectable per-testpoint, to separate voltage references per board

High Impedance Terminator Voltage Range

0 V to +5.1

High impedance Terminator Voltage Setting Resolution

20 mV

High Impedance Terminator Resistance

4.45 KΩ + 15%

High Impedance Terminator Voltage Accuracy

+3.9% + 60 mV

Low Impedance Terminator Voltage Range

0 V to +5.1 V or programmed Driver Vcc if lower. Maximum continuous dissipation 0.25Ω per testpoint

Low Impedance Terminator Voltage Setting Resolution

20 mV

Low Impedance Terminator Resistance

1000 + 15%

Low Impedance Terminator Voltage Accuracy

+ 0.9% + 65 mV

SYSTEM SOFTWARE

Aeroflex Integrated Development Environment (AIDE)

High level, method based, structured programming language

Interactive edit and debug facilities

Included packages:-

DLL Wrapper tool

System self check

Computer Assisted Program Generation (CAPG)

Generic device library

CAD or manual input

Multi-board

i-Base5 Data Collection and Analysis System (option)

GENERAL

FIXTURE INTERFACE

Programmable Fixture Relays

20 single pole relays with a contact rating of 0.5 A max. (10 W max switching power)

Resistance 0.5 Ω ±0.18 Ω

Programmable Fixture Control lines

12 open drain outputs. +25 V max. OFF.

<0.1 V max at 100 mA max. ON.

Fixture Ident

16 bit Fixture identification code. LVTTL input with 10 KΩ in series and 10 KΩ to +3.3 V pull-up.

Fixture Sense Inputs

8 inputs, Fixture sense input to system. LVTTL input with 10 KΩ in series and 10 KΩ to +3.3 V pull-up.

Fixture Type Inputs

8 inputs, Fixture type input to system. LVTTL input with 10 KΩ in series and 10 KΩ to +3.3 V pull-up.

Fixture Data Output

Outputs, Fixture data output from system. LVTTL outputs.

Fixture Power (standard)

+5 VSW	*+5 V, unregulated, 1 A, switched*
+15 VSW	*+15 V, 100 mA, switched.*
-15 VSW	*-15 V, 100 mA, switched.*
+5 V	*+5 V, 5 A, switched*
+15 V	*+15 V, 2 A, switched.*
-15 V	*-15 V, 2 A, switched.*
+24 V	*+24 V, 2 A, switched.*

USER POWER SUPPLIES

Programmable UUT PSUs

Two types of user supplies are available, a dual and a single output unit. Each user power supply is voltage and current limit programmable with both Voltage and Current read back via the system software.

Power Output

Floating output

VOLTAGE OUTPUT

Range

0 V to 15.0 V / 0.001 A to 5 A

0 V to 35.0 V / 0.001 A to 3 A

Resolution

1 mV

Accuracy

±(0.03% + 5 mV)

Maximum Current

5 A

Ripple and Noise

<0.35 mV rms and 2 mVp-p (20 MHz bandwidth)

CURRENT LIMIT

Range

0.01 A to 5.5 A

Resolution

0.01 A

Output Protection

Output will withstand forward voltages of up to 20 V above rated output voltage. Reverse protection by diode clamp for currents up to 3 A.

OPERATING CONDITIONS

Mains Supply

100 - 240 V, 50 - 60 Hz, single phase 13 amps max. (5820/5830)

100 - 240 V, 50 - 60 Hz, single phase 20 amps max. (5860)

Operating Temperature Range

+10°C - +35°C

Temperature Gradient

10°C/hour

Humidity Range

25% RH - 75% RH, maximum dry bulb +30°C

Humidity Gradient

12% RH/hour

Dimensions

		Height	Depth	Width
5820/5830		0.42 m	0.58 m	0.48 m
5860	Flat Bed	1.25 m*	0.90 m	0.60 m
5860	Upright	1.35 m	0.90 m	0.60 m

** - Includes monitor pole*

Weight (will depend on system configuration)

5820/5830

40 - 48 Kg

5860

<150 Kg

CHINA Beijing
Tel: [+86] (10) 6539 1166
Fax: [+86] (10) 6539 1778

CHINA Shanghai
Tel: [+86] 21 2028 3588
Fax: [+86] 21 2028 3558

CHINA Shenzhen
Tel: [+86] (755) 3301 9358
Fax: [+86] (755) 3301 9356

FRANCE
Tel: [+33] 1 60 79 96 00
Fax: [+33] 1 60 77 69 22

GERMANY
Tel: [+49] 89 99641 0
Fax: [+49] 89 99641 160

HONG KONG
Tel: [+852] 2832 7988
Fax: [+852] 2834 5364

INDIA
Tel: [+91] 80 [4] 115 4501
Fax: [+91] 80 [4] 115 4502

JAPAN
Tel: [+81] (3) 3500 5591
Fax: [+81] (3) 3500 5592

KOREA
Tel: [+82] (2) 3424 2719
Fax: [+82] (2) 3424 8620

SCANDINAVIA
Tel: [+45] 9614 0045
Fax: [+45] 9614 0047

SINGAPORE
Tel: [+65] 6873 0991
Fax: [+65] 6873 0992

TAIWAN
Tel: [+886] 2 2698 8058
Fax: [+886] 2 2698 8050

UK Stevenage
Tel: [+44] (0) 1438 742200
Fax: [+44] (0) 1438 727601
Freephone: 0800 282388

USA
Tel: [+1] (316) 522 4981
Fax: [+1] (316) 522 1360
Toll Free: 800 835 2352

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www.aeroflex.com

info-test@aeroflex.com

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Part No. 46891/258, Issue 5,10/12