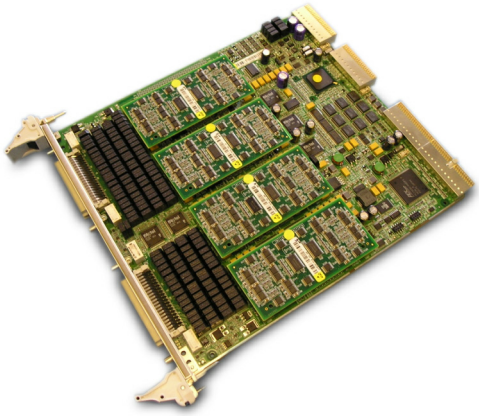
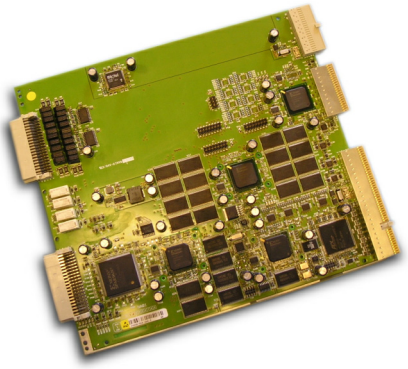
ATE

5800 Series Digital Functional Test System





The Digital Functional sub-system comprises a Digital Test Controller (DTC) card, together with up to 18 Digital Testpoint (DTP) cards.

- Protocol Emulation
- Device Programming
- 4 x 16 bit Pattern Generators
- 64 non-multiplexed drive/sense channels per DTP card
- Programmable Logic Levels
- Up to 16 k memory per channel
- Relay isolation on all channels
- Analog signal routing

Introduction

When engineers think of digital test, they usually envisage an application that either generates or acquires a pattern of 1's and 0's to communicate with or test a device under test (DUT). Changes in recent digital components, which include faster speeds, new logic families, and smaller packaging, require more data throughput on fewer pins. These changes require a digital tester to support more operations than just the two basic states, drive logic low and drive logic high.

In addition, current digital electronics, from simple memory chips to complex communication systems, require a flexible, powerful digital test solution to reduce the cost and time of interfacing to a wide range of electronic technologies.

The 5800 Series Digital Functional sub-system can perform operations that include driving flexible voltage levels, disabling circuitry, bi-directional communication, and analyzing the acquired data for accuracy.

MODULE FUNCTIONALITY

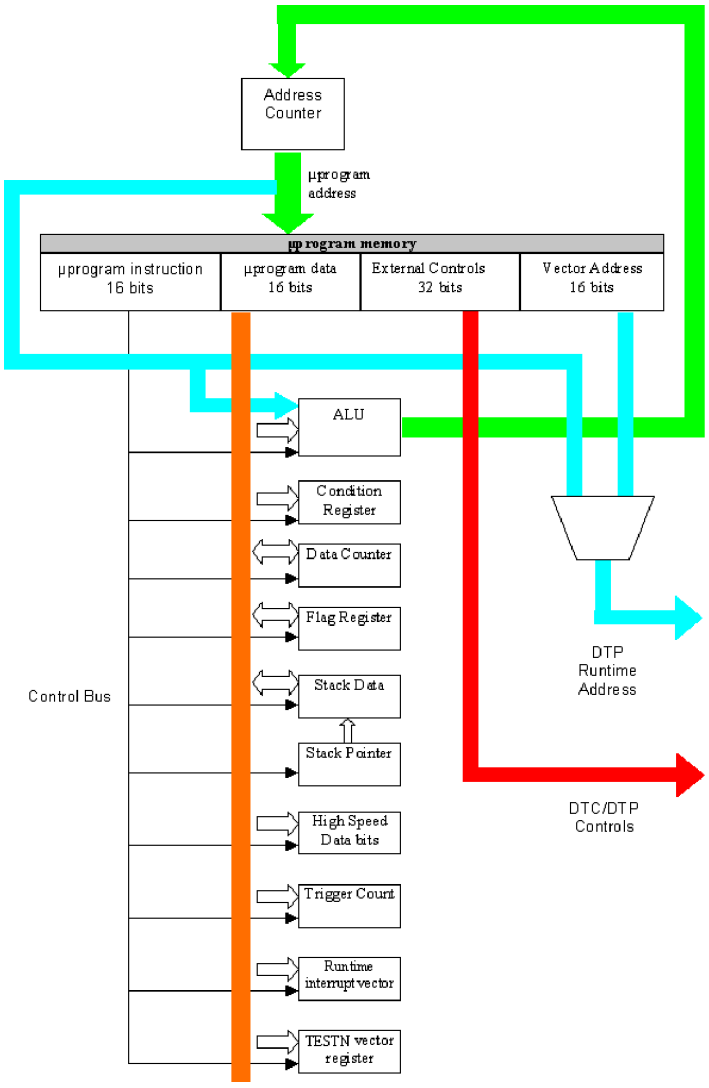
Digital Test Controller (DTC) card

The Digital Functional sub-system of the 5800 Series of testers is made up of a DTC card and up to 18 DTP cards. The DTC may plug in to any of slots 3-21 of the system backplane and interfaces with both the PXI backplane and system backplane (see 5800 datasheet). There is no preferred slot, although the board should be positioned to the left of a group of DTP cards (as viewed from the front).

The DTC contains a sequencer, which controls execution of a digital test independent of the host PC. Configuration data and the test sequence are set up on the DTC card and the test is then started. From this point, the DTC controls the activity of the DTP cards via the system backplane until the test is complete. The DTC can also pause to allow other test activity (e.g. analog tests) to be performed or can trigger execution of analog tests while maintaining digital testpoint activity.

A single-step mode is available where runtime operation is paused at the end of each test step, but each instruction is executed at full speed using pin formats and timing. For very simple digital tests, the DTP testpoints can also be operated directly under software control.

The DTC has an internal clock speed of 200 MHz, allowing vector rates of 10 MHz with 5 ns edge placement, this specification allows comprehensive testing of the most complex and demanding devices today.



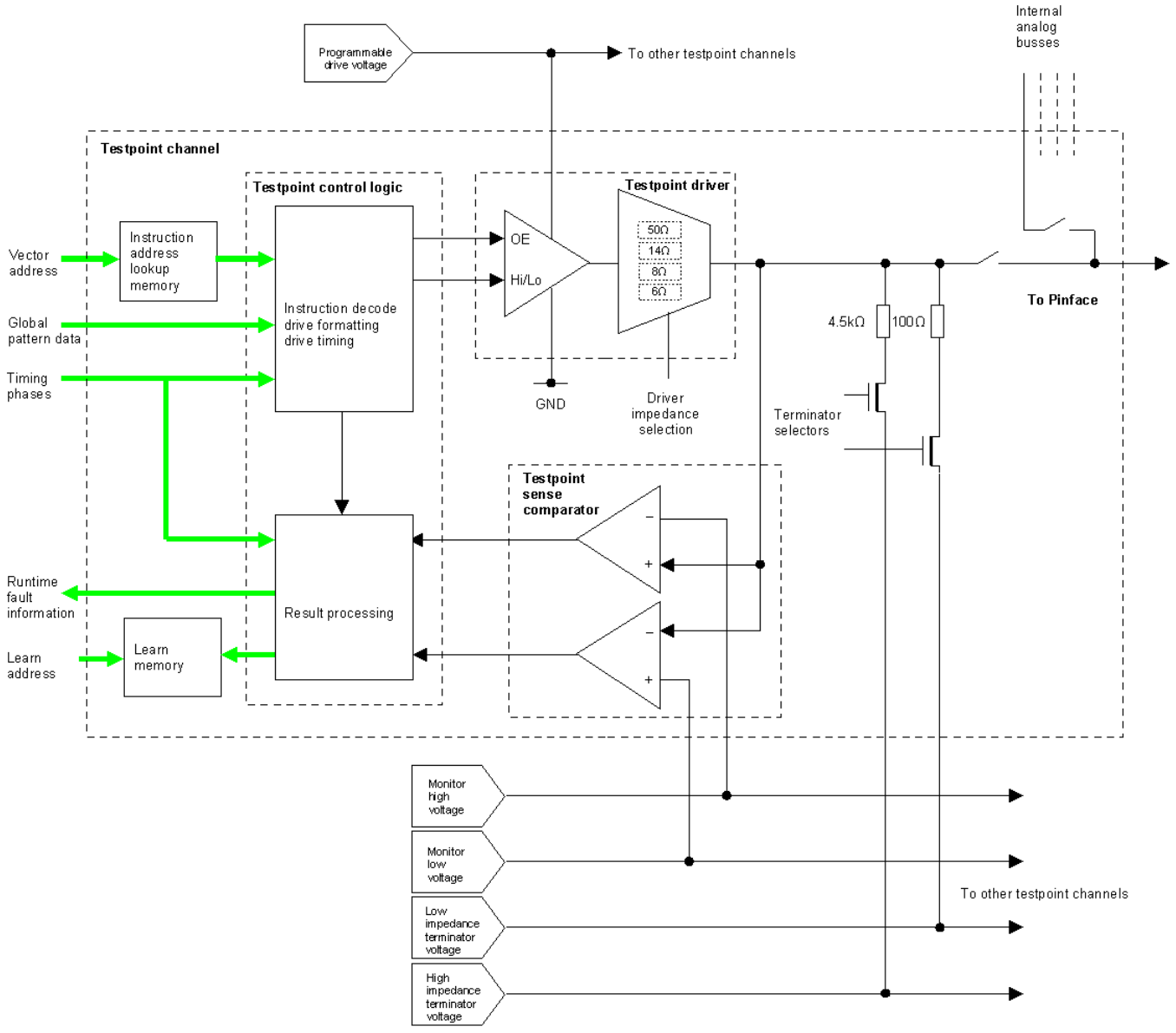
Digital Test Controller

The 5800 digital test system also includes a range of advanced features, such as internal hardware and PXI triggers, pin formatting and variable timing sets. The On-the-fly jumps allow for program flow decisions to be made not only within the test program but also in real-time within an individual digital test.

Digital Testpoint (DTP) cards

The DTP has 64 non-multiplexed functional drive/sense channels that are relay-isolated to the fixture interface connectors allowing a maximum digital test point count of 1152.

Every testpoint of the digital sub-system has the ability to switch between a digital & analog resource, this is a key feature when testing mixed signal devices such as ADCs, DACs etc or performing analog in-circuit tests. Every testpoint is provided with terminator circuitry to enable testing of tristate buses and open collector devices. The skew for both drive and the sense channel of any given testpoint is carefully controlled to ensure the test vectors delivered to the tester interface are of the highest integrity.



Single Digital Testpoint channel

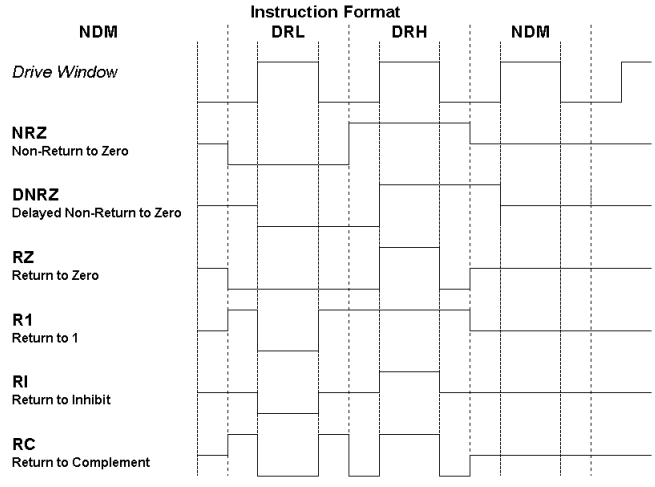
Instruction Address Lookup Memory

The testpoint instruction RAM contains an index to a set of instructions stored in an array for each testpoint or testpoint block of 16. A default set of DTP instructions are provided, but the flexibility of this arrangement allows for new instructions to be created as required.

There are 6 instruction formats (NRZ, DNRZ, RI, RC, RZ, R1) which along with the instruction set determine testpoint driver behaviour within a test step (see below). Instruction formats are selectable at non-runtime on a per testpoint basis and may be changed at run time as part of an instruction.

Default Testpoint Instruction Set

NDM	No Drive Monitor (Off).
NOCH	A repeat of the previous pinface drive and monitor action.
DRL	Drive low.
DRH	Drive High.
DRP	Drive Pattern - the polarity of the selected pattern generator bit determines the drive sense (high or low).
DML	Drive and monitor low - the drive is verified.
DMH	Drive and monitor high.
DMP	Drive monitor pattern.
MNL	Monitor low.
MNH	Monitor high.
MNZ	Monitor tristate.
MNP	Monitor pattern.
TSTL	Test Low - result goes to the EVENT line not the FAULT line.
TSTH	Test High.
TSTZ	Test tristate.
TSTP	Test Pattern.
TOG	Toggle - polarity of pinface drive and monitor is inverted, driver output state (on or off) is unchanged.



Data is stored in the instruction memory in a compressed form, making efficient use of its size. This is achieved by only storing those test vectors that have changed, rather than the states of the pins at each test step.

Learn Memory

Instruction and pinface activity are combined into a learn code for each testpoint, which is written on each test step that learn is enabled. The learn RAM may be used to record the output of the testpoint monitor comparator pairs, allowing tristate conditions to be detected.

An example of the use for this facility are Audio RAM chips. Audio RAM specifications usually allow for a number of faults to occur within a device, providing that there are no adjacent addresses that are faulty. Using the learn RAM the occurrence and position of failing addresses can be logged. The learn RAM can then be interrogated at the end of the device test to determine whether the device has failed the specification.

Testpoint Drive and Sense

Reference Voltages

Each DTP card contains 5 programmable reference supplies to set the logic drive level, the monitor high & low thresholds, together with the high & low impedance terminator voltages.

Sense Comparators

Each testpoint monitor circuit consists of 2 comparators, for comparison against the high and low references. The comparator outputs are combined with monitor instruction and selected timing line to generate fault information.

Testpoint Terminators

The DTP card has a high and low impedance terminator per testpoint. The high impedance terminator is intended to pull UUT tristate outputs to a defined state, the low impedance terminator is mainly for controlling transmission line effects on signals driven by the UUT.

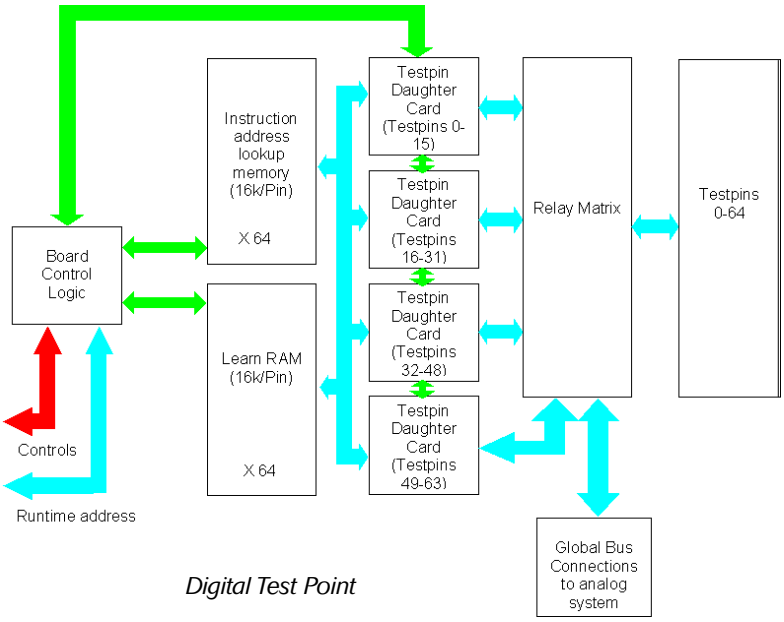
Analog routing

Connect to a single or multiple internal busses with 1 relay per pin, with a small matrix to the global analog bus: Each board has analog access via a relay on each test point, allowing all AIDE in-circuit and UUT tests to use DTP testpins.

Architecture

The DTP card architecture comprises of 64 identical testpoint channels as shown above, that are further divided in to 4 elements consisting of: -

- Control FPGA
- 16-bit wide instruction memory
- 16-bit wide learn memory
- 16-channel drive and sense logic (some of which is partitioned on to a daughter board)
- Testpoint terminators
- 16 isolation relays, and 16 relays to internal busses



Digital Test Point

Digital Functional Software Environment

A digital test consists of parallel sets of drive and sense patterns applied to the test subject to verify correct operation under control of the DTC microprogram sequencer.

```
Method IC12 [ ] ( )
  Local Symbols
  Method Code
    Digital Module Clock = Internal, 1us
      Digital Configuration Data
      Digital Variables
      Code
        Digital Test Block
          STEP DNBL DML(CLEAR, CLK) DMH(LOAD) MNL(QBus)
          STEP DMH(CLEAR) CLOCK_PG(Q) Comment = "clock pg(Q) to preload count 1"
          Comment "Count (note no access to Qd)"
          REPEAT count Times
          Comment "Test parallel load"
          STEP DML(LOAD) NDM(QBus)
          STEP DRH(CLK) MNB(QBus=4)
          Comment "Test master reset"
          STEP DML(CLEAR) MNB(QBus=0)
          STOP 0
        Digital Test IC12 DeviceID = IC12
```

Pattern generators allow the test engineer to program address data into a block of memory, this can then be used in conjunction with the CRC (Cyclic Redundancy Checks) hardware in order to carry out Signature Analysis on devices.

When programming a device the pattern generators are loaded with the data to be programmed. This data could be within the test program, or stored separately on a disk. The method chosen depends on the volume of data to be programmed. Generally it is more appropriate to store large amounts of data in an external file. The pattern generators then download the data to the device under test. All of this procedure is executed using Aeroflex Integrated Development Environment (AIDE) therefore powerful operations are executed with simple instructions.

The DTC supplies 64 bits of pattern generator data along the system backplane for use on the DTP cards to control the activity on selected testpoints. The 64 bits are sourced from a set of 4 16-bit pattern generators. Each pattern generator consists of a block of RAM, addressed by a configurable counter. The counters have programmable count lengths, and may be cascaded together to generate wider/longer counts. The RAM is loaded with the required test pattern before the start of a test run.

Parallel outputs from the generator may optionally be converted into serial data and transmitted along the backplane lines, which may similarly be used as a source of DTP instruction data.

Timing set data are transmitted on the backplane to the DTP boards, along 8 physical timing lines. Timing line selection is per-testpoint, selectable at non-runtime and may be changed at run time as part of an instruction.

Boundary Scan

The 5800 Series Digital Functional sub-system fully supports the IEEE1149.4 boundary scan standard and integrates with both JTAG Technologies and Goepel platforms. Integration is achieved through the use of the supplied controller card (PXI, PCI etc.) and associated interconnects, thus allowing boundary scan test programs to be executed under the control of the AIDE environment. The advantage of this is that programs that have been developed for the debugging of new designs or for bench testing of prototypes can now be re-used in production test.

During the execution of the boundary scan program, the DTP can be added to the boundary scan chain and used to provide external stimulus to the UUT in order to effect the behavor of peripheral components (disable or configure device etc.). AIDE handles the resultant fault reporting transparently, giving a totally integrated run time solution.

SPECIFICATION

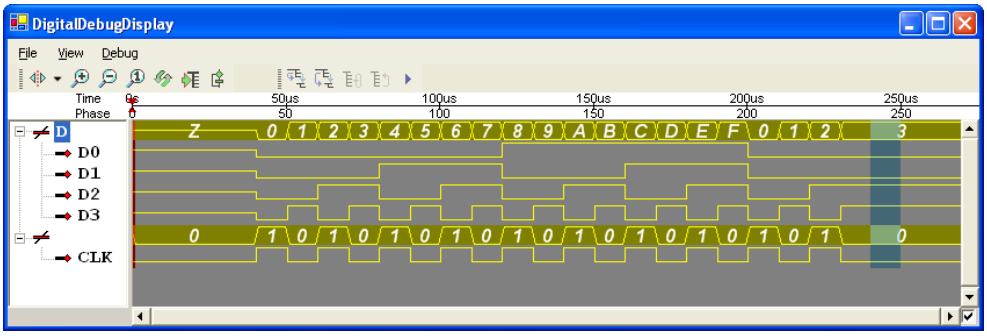
DIGITAL TESTING

General Capability

Microprogram sequencer memory depth	*64k test steps, each test step consists of a programmable number of sub-steps from 4-512*
Microprogram control instructions	*Instruction set includes: jump, loop, subroutine call/return, repeat, delay, conditional operations, pause, stop. Single step operation available.*
Test step period	*100 ns min (10 MHz test step rate), with increments of 5 ns, or synchronized to external clock from the UUT.*
Edge placement resolution	*5 ns min*
Sub-step length	*Sub-step length is a programmable number of master clock periods. Each master clock period is 5ns (internal clock), or dependent on an external clock routed via PLL clock generator which provides programmable multiply and divide ratios.*
Sub-step timing	*There are 16 sets of user-programmable waveforms that may be applied to 8 physical timing lines. Each set of waveforms is known as a timing set. Timing sets are selectable at runtime, from microprogram instruction. Each physical line is selectable for use as drive or sense, but not both, for a particular test run. Minimum pulse width per timing line is 20 ns.*
Data compression	*16-bit indirect vector address applied to DTP cards.*
Pattern generators	*4 software-loadable pattern generators on DTC (global resource), each with 1 M x 16 RAM. Pattern generators have variable count length, and may be linked to generate up to 64 bit-wide pattern. Pattern generator data may also be serialized (16:1 or 64:1) and transmitted along 4 GPIO lines for use by the DTP, giving up to 64 M-bit long pattern without reload.*
Trace Ram	*For tracing program flow. 256 k locations, compressed.*
Triggers	*Access to the PXI trigger bus is provided.*

Internal master clock

Accuracy	*200 MHz + 0.1%*



Digital Debug

External clock

The external clock input is routed via a clock generator with programmable multiply/divide ratios to generate a higher or lower frequency than the external clock. The resultant intermediate clock is multiplied by 4 to generate the master clock.

Number of input channels	*4*
Input frequency range	*2 MHz - 50 MHz*
Input type	*LVTTL input, 100 R series resistor and 10 kR pullup to +3.3 V.*
Input voltage range	*0 - 5.5 V*
Termination	*50Ω || 10pF or none, relay selectable*
Polarity	*Selectable high or low*
Delay	*8-bit programmable, 0.5 ns per bit*

External sync A/B inputs

Two sync input circuits (A/B) are provided. When programmed for external sync, runtime activity is held until the programmed sync input is set active from the UUT.

Number of input channels	*4*
Input type	*LVTTL input, 100 R series resistor and 10 kR pullup to +3.3 V.*
Input voltage range	*0 - 5.5V*
Termination	*50 Ω || 10 pF or none, relay selectable*
Polarity	*Selectable high or low*
Triggering	*Level sensitive*

External event input

An input to the condition logic that may be used to control conditional program flow.

Number of input channels	*4*
Input type	*LVTTL input, 100 R series resistor and 10 kR pullup to +3.3 V.*
Input voltage range	*0 - 5.5 V*
Termination	*50 Ω || 10 pF or none, relay selectable*
Triggering	*Level sensitive*

DIGITAL TESTPOINT CARD (DTP)

General capability

Analog routing	*Connect to a single or multiple internal busses with 1 relay per testpoint, with a matrix to the global analog bus.*
Immediate mode	*Immediate mode operation is available, where drive and sense operations can be programmed independent of the DTC microprogram controller.*
Boundary scan	*A boundary scan mode is available, where the testpoints may be included in a boundary scan path on the UUT.*
Fixture I/O FPDx	*A set of digital inputs to the testpoint control logic, may be used as a source of pattern data, or as part of the boundary scan port when the board is used in boundary scan mode. LVCMOS level inputs, with 470R series resistors and pull-up/down resistors:*
	FPD0, FPD2 10 kΩ to GND
	FPD1, FPD3 10 kΩ to 3.3V
Fixture boundary scan TDO	*FTDO signal, used when the board is in boundary scan mode. LVCMOS output.*
Fixture grounds	*Both switched and fixed grounds are available at the interface connectors.*

Digital Testpoint characteristics

Testpoint instruction memory	*16k x 4 bits per testpoint, addressed at runtime by the DTC microprogram vector address. Each instruction memory location contains an index to the testpoint instruction arrays, which are 64-bits wide per-testpoint. This allows complex and variable instruction sets to be created.*
Testpoint learn memory	*16k x 4 bits per testpoint*
Testpoint skew	*±10 ns maximum skew between any 2 testpoints, driving or monitoring, when programmed to the same drive voltage level and drive strength and under no-load conditions. Skew specification applies at the interface connectors, and does not include additional effects of cables.*
Maximum input voltage	*±100 V logic relay open*
	Drive High Voltage logic relay closed
Stray capacitance	*150 pF maximum, to GND, driver off, logic relay closed*
	50 pF maximum to GND, logic relay open
	5 pF maximum to adjacent testpoint, logic relay open
	400 pF maximum to GND, relay to internal analog bus closed
Leakage current into analog bus lines	*20 nA maximum per analog bus line*
Resistance to GND	*100 MΩ to GND, logic relay open*
Relay switch current	*500 mA, 10 W switching power maximum*
Relay carry current	*500 mA maximum*

Testpoint driver specification

Driver Vcc range	*2 V to 5.1 V*
Driver Vcc resolution	*15 mV*
Formats per testpoint	*Non-return to Zero (NRZ)*
	Return to Zero (RZ)
	Return to 1 (R1)
	Return to Inhibit (RI)
	Return to Complement (RC)
	Delayed Non-Return to Zero (DNRZ)
Drive strength	*4 selectable drive strengths, 50 Ω, 14 Ω, 8 Ω, 6 Ω nominal output impedance*
Driver Level Accuracy	*±3.7% ±75 mV*

Maximum Drive Low Voltage	***Drive High Voltage = 3.0 V***
	0.5 V
	5.5 mA load, 50 Ω output impedance
	17 mA load, 14 Ω output impedance
	27 mA load, 8 Ω output impedance
	37 mA load, 6 Ω output impedance
	Drive High Voltage = 4.5 V
	0.5 V
	7.5 mA load, 50 Ω output impedance
	29 mA load, 14 Ω output impedance
	48 mA load, 8 Ω output impedance
	65 mA load, 6 Ω output impedance
Minimum Drive High Voltage	***Drive High Voltage= 3.0 V***
	2.7 V
	50 uA load, all drive strengths
	2.26 V
	6 mA load, 50 Ω output impedance
	17 mA load, 14 Ω output impedance
	28 mA load, 8 Ω output impedance
	38 mA load, 6 Ω output impedance
	Drive High Voltage = 4.5 V
	4.2 V
	50 uA load, all drive strengths
	3.56 V
	11 mA load, 50 Ω output impedance
	33 mA load, 14 Ω output impedance
	54 mA load, 8 Ω output impedance
	73 mA load, 6 Ω output impedance
Driver output current	***Continuous***
	25 mA, 50 Ω output impedance
	50 mA, 14 Ω output impedance
	75 mA, 8 Ω output impedance
	100 mA, 6 Ω output impedance
	Dynamic
	30 mA, 50 Ω output impedance
	100 mA, 14 Ω output impedance
	175 mA, 8 Ω output impedance
	250 mA, 6 Ω output impedance

Driver Output Impedance (Nominal 6 R)	***Accuracy***	***2.0 V***	***3.3 V***	***5.0 V***
		8.5R ±5.0R	*5R ±3.5R*	*3.5R ±2.9R*
Driver Output Impedance (Nominal 8 R)	***Accuracy***	***2.0 V***	***3.3 V***	***5.0 V***
		11.5R ±7.2R	*7R ±4.3R*	*5R ±3.5R*
Driver Output Impedance (Nominal 14 R)	***Accuracy***	***2.0 V***	***3.3 V***	***5.0 V***
		20R ±9.1R	*12R ±6.1R*	*9R ±5R*
Driver Output Impedance (Nominal 50 R)	***Accuracy***	***2.0 V***	***3.3 V***	***5.0 V***
		65R ±21R	*50R ±13R*	*45R ±12R*

Testpoint monitor specification	
Voltage range	*0 V to +5.1 V*
Accuracy	*±3.9% ±65 mV*
Reference setting resolution	*20 mV*
Input impedance	*20 kΩ ±10% terminators off*
Testpoint terminator specification	*High and low impedance terminator re selectable per-testpoint, to separate voltage references per board*
High impedance terminator voltage range	*0 V to + 5.1 V*
High impedance terminator voltage setting resolution	*20 mV*
High impedance terminator resistance	*4.45 kΩ ±15%*
High impedance terminator voltage accuracy	*±3.9% ±60 mV*
Low impedance terminator voltage range	*0 V to +5.1 V or programmed Driver Vcc if lower. Maximum continuous dissipation 0.25 W per testpoint*
Low impedance terminator voltage setting resolution	*20 mV*
Low impedance terminator resistance	*100 Ω ±15%*
Low impedance terminator voltage accuracy	*±0.9% ±65 mV*

CHINA Beijing
Tel: [+86] (10) 6539 1166
Fax: [+86] (10) 6539 1778

CHINA Shanghai
Tel: [+86] (21) 5109 5128
Fax: [+86] (21) 5150 6112

FINLAND
Tel: [+358] (9) 2709 5541
Fax: [+358] (9) 804 2441

FRANCE
Tel: [+33] 1 60 79 96 00
Fax: [+33] 1 60 77 69 22

GERMANY
Tel: [+49] 8131 2926-0
Fax: [+49] 8131 2926-130

HONG KONG
Tel: [+852] 2832 7988
Fax: [+852] 2834 5364

INDIA
Tel: [+91] 80 5115 4501
Fax: [+91] 80 5115 4502

KOREA
Tel: [+82] (2) 3424 2719
Fax: [+82] (2) 3424 8620

SCANDINAVIA
Tel: [+45] 9614 0045
Fax: [+45] 9614 0047

SPAIN
Tel: [+34] (91) 640 11 34
Fax: [+34] (91) 640 06 40

UK Burnham
Tel: [+44] (0) 1628 604455
Fax: [+44] (0) 1628 662017

UK Cambridge
Tel: [+44] (0) 1763 262277
Fax: [+44] (0) 1763 285353

UK Stevenage
Tel: [+44] (0) 1438 742200
Fax: [+44] (0) 1438 727601
Freephone: 0800 282388

USA
Tel: [+1] (316) 522 4981
Fax: [+1] (316) 522 1360
Toll Free: 800 835 2352

AEROFLEX
A passion for performance.

www.aeroflex.com
info-test@aeroflex.com

Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused.

Part No. 46891/305, Issue 1, 11/07