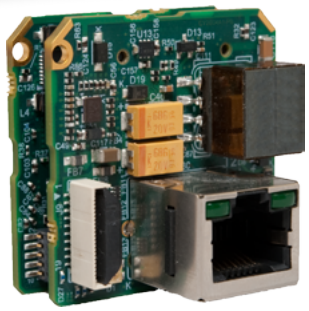
DATA SHEET

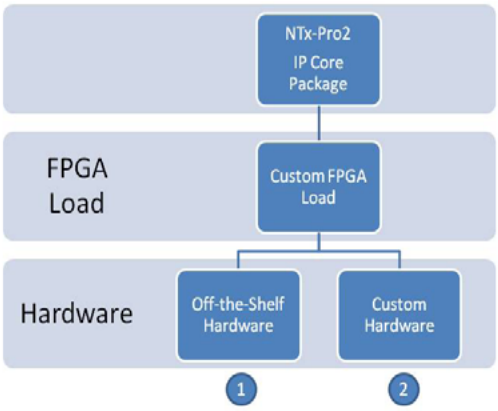


iPORT™ NTx-Pro2 IP Core Package

The iPORT NTx-Pro2 IP Core Package gives you the option to design GigE Vision compliant FPGA loads that incorporate custom logic, while leveraging either off-the-shelf or custom hardware.

Develop Your Own FPGA Loads

With the iPORT NTx-Pro2 IP Core Package, which includes our HDL Reference Design, you have maximum design flexibility while being supported by our team of experts.



Option 1:

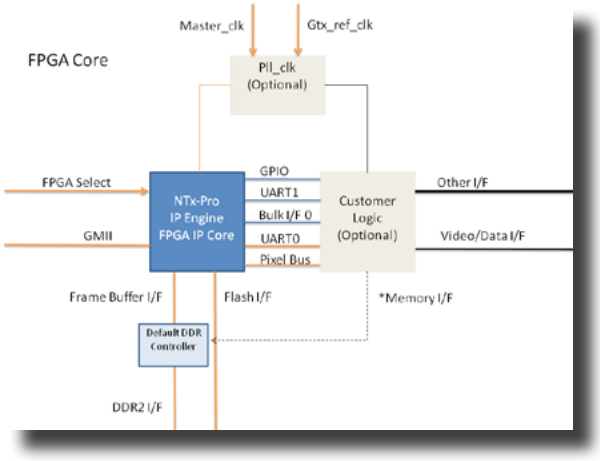
Leverage off-the-shelf NTx-Pro2 IP engine hardware while customizing the content of the FPGA by integrating the NTx-Pro2 IP core with your own logic, with the option to use Pleora's HDL Reference Design. This integration scenario provides fast-time-to-market and design flexibility at relatively low risk. You need to include some engineering time in your schedule to integrate your own FPGA logic.

Option 2:

Develop your own hardware by following the Hardware Reference Design, licensed by Pleora. Then, create a custom FPGA load by integrating the NTx-Pro2 IP core with your own logic, with the option to use Pleora's HDL Reference Design. More engineering time is required to implement your own hardware and FPGA, but option 2 provides maximum design flexibility, and can reduce PCB real estate, the parts list, and power consumption—thereby giving you a fully optimized solution.

Creating a Custom FPGA Load

If the off-the-shelf FPGA load does not meet your specific needs, you can integrate the NTx-Pro2 IP core with your in-house logic to function together in a single FPGA.



GiGE VISION

GEN<i>CAM

For more information, visit
www.pleora.com/our-products/iport-video-transmitters/iport-ntx-pro-intellectual-property/iport-ntx-pro2-ip-core-pac

Pleora Technologies

iPORT™ NTx-Pro2 IP Core Package

Benefits of a Custom FPGA Load

Combining Pleora's and your own custom logic onto a single FPGA can provide a multitude of benefits—lower power consumption, lower heat generation, smaller product size, lower cost, and higher reliability. You can create a single FPGA load that can perform custom pixel correction, color space conversion, or other transformation or analysis, before sending images to Pleora's NTx-Pro2 IP core.

Your custom logic can communicate with other external devices by making use of the UART or BULK serial data links, which connect your logic to the network using the GigE Vision standard. If a simpler communication method is desired, a GPIO (General Purpose Inputs and Outputs) interface is also provided with the IP Core Package.

In addition to the FPGA, you can choose to share the same Flash memory or non-volatile memory used by Pleora's IP core.

Pleora's HDL Reference Design helps speed time-to-market even further by providing pin mappings for the key external interfaces, when you use an Altera Cyclone III FPGA (EP3C55F324 or EP3C40F324).

FPGA Resource Consumption

Examples of the FPGA resources consumed by the NTx-Pro2 IP Core Package (including HDL Reference Design) are shown in the table below:

FPGA	Grade	LEs*	Memory blocks (M9k)	PLLs	DSP Blocks (Multipliers)
Cyclone III EP3C40F324	C8	18378	37	2	2
Cyclone III EP3C55F324	C8	18378	37	2	2

* Logic Elements

NTx-Pro2 IP Core Package Feature Summary

Feature	Description
User Circuitry Interface	• De-serialized Camera Link® (Pixel Bus)
FPGA Supported by IP Core	• Altera Cyclone III • Altera Cyclone III LS • Altera Cyclone IV (E and GX)
FPGA Load	• User defined to GigE Vision load created by customer, based on the Pleora IP core • Default or customized backup load
HDL Reference Design	• Verilog
Image Buffer (DDR)	• 16-bit wide • 32 MB (256 Mb) DDR2 RAM The IP core requires the first 32 MB of the frame buffer, leaving the remaining available space available for your custom logic.
FPGA/PHY I/F	• GMII or RGMII
PHY	• Broadcom BCM5461 • Broadcom BCM5461S • Marvell 88E1310S
FPGA External Memory	• PSRAM: • 4MB (Micron MT45W2MW16PDGA -70W)
FPGA Configuration Controller	• None
Persistent Memory	• 16-bit wide Parallel FLASH • 128 Mbit: Micron part PF48F3000P0ZBQ • 256 Mbit: Micron part PF48F4000P0ZBQ (preferred) To ensure compatibility with future firmware loads or upgrades, you should use the 256 Mbit version.
Power Supply and Reset Generator	• Optional • NTx-Pro2 power supply and reset generator included in the Hardware Reference Design kit
GPIO Inputs/Outputs	• 4 x 2.5V LVTTL
Clock Generator	• Included
Boundary Scan Chain	• All ICs
Serial communication	• 2 UART and 1 BULK (USRT)

Pleora Technologies Inc.
359 Terry Fox Drive, Suite 230
Kanata, Ontario
Canada, K2K 2E7

Tel: +1.613.270.0625
Fax: +1.613.270.1425
Email: info@pleora.com
www.pleora.com