E100 Chimera

100Gbps 5-speed, 2 port QSFP28 network emulation module

Key Features

- Industry's only fully integrated Ethernet traffic generation & impairment solution

- Multi-speed impairment– 10/25/40/50 & 100GE – in a compact 1U chassis or as a B2400 test module

- High port density

- Flexible port reservation

E100 Chimera can emulate network impairment at five Ethernet speeds: 100GE, 50GE, 40GE, 25GE and 10GE

This flexibility is provided via two physical transceiver cages that both support QSFP28 and QSFP+ transceivers.

The result is a versatile solution that provides consistent, accurate, well-defined and repeatable impairments to traffic between DUTs in the lab. E100 Chimera is ideal for benchmarking, stress/negative, "what-if" and regression testing of network infrastructure and Ethernet equipment capable of supporting 100GE such as switches, routers, NICs and fronthaul/backhaul platforms.

A unique feature of the E100 Chimera is it works seamlessly with the Xena traffic generators allowing test engineers to both generate traffic and add impairments to it via the same GUI.

E100 Chimera is easily controlled using XOA CLI scripting, making automation of tests simple using the Python library supplied by Xena.

E100 Chimera can test five speeds up to 100GE and is available in the standalone desktop chassis or as a 1-slot test module for the Xena B2400 chassis.

Find out more here:

SYSTEM OVERVIEW	
Interface category	QSFP28 100G, 50G, 40G*, 25GE and 10G* Ethernet QSFP+ 40G, 10G Ethernet * Depending on transceiver capabilities
Total number of test ports (software configurable)	2x100G, 4x50G, 2x40G, 8x25G and 8x10G Ethernet
Interface options	Each cage • 1 x 100GBASE-SR4/LR4/CR4, or 802.3bj standard • 2 x 50GBASE-SR2/LR2/CR2, or Consortium** • 1 x 40GBASE-SR4/LR4/CR4, or 802.3ba • 4 x 25GBASE-SR/LR/CR, or 802.3by/Consortium** • 4 x 10GBASE-SR/LR/CR 802.3ae Actual interface options depend on the capabilities of the inserted transceiver. Both cages must run with the same base interface configuration (e.g. 2 x 50G). ** As defined by the Ethernet Technology Consortium
Forward Error Correction (FEC)	• RS-FEC (Reed Solomon) FEC, IEEE 802.3 Clause 91 (100GE) • RS-FEC (Reed Solomon) FEC, IEEE 802.3 Clause 108 (25GE) • RS-FEC (Reed Solomon) FEC, 25G Ethernet Consortium (25GE)
Number of transceiver module cages	2 x QSFP28/QSFP+
Port statistics	Link state, FCS errors, frame and byte counters
Field upgradeable	System is fully field upgradeable to product releases (FPGA images and software)
Tx disable	Enable/disable of optical laser
SyncE	Lock Tx clock to recovered Rx clock from any input port (Single clock domain)
Emulator bypass mode	Sub 1 µs delay (depending on port speed) ability is +/- 35 ppm)

(*) Depends on speed variant. See Ordering Information.

| 100/50/40/25/10GE PCS/PMA LAYERS	
Link Flap	Single short or repeatable link down events with ms precision
Error Injection (PMA Layer)	Single short or repeatable error inject periods at PMA layer with ms precision
Supported frame sizes	Ethernet packets from 56 to 12288 bytes

FLOWS	
Number of flows per port	8 (incl. default flow)
Flow filter definition	Any protocol within the first 128 packet bytes. This includes: • Ethernet (DMAC / SMAC) • Any number of VLAN tags. • Any number of MPLS labels. • IPv4 / IPV6 • UDP/TCP • eCPRI / RoE • Custom data fields. • Xena Payload ID (Xena proprietary)
Flow statistics	E100q Chimera implements impairment counters per flow, including dropped, corrupted, mis-ordered and duplicated packets.

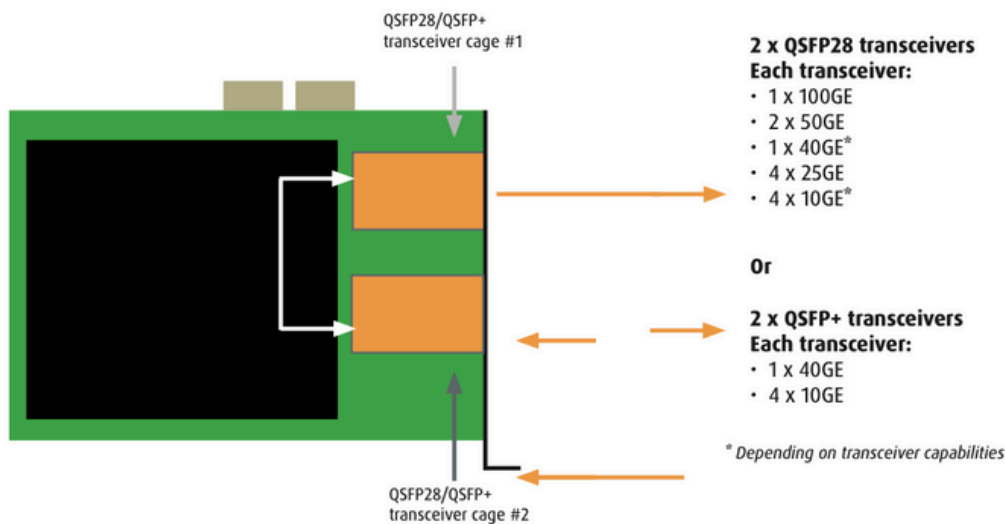| IMPAIRMENT PER FLOW	
General	Impairments can be changed dynamically
Packet Manipulation	Packet drop Duplication Mis-ordering Protocol Corruption (Ethernet Frame FCS, IP/UDP/TCP header Check Sum error)

Latency / Jitter	• Max. latency lossless 399 ms (100GE wire-speed)
	• Step-size 100 ns, accuracy: +/- 50 ns
	• Max. latency reduced bandwidth: 19.5 sec
	• Min. (Intrinsic) delay:
	   ○ 7.1 µs for 40G/50G/100G
	   ○ 7.3 µs for 25G
	   ○ 13.0 µs for 10G

Latency / Jitter Distribution	Latency impairments can be applied with very flexible distributions including:
	   Constant
	   Accumulate Burst
	   Step (2 alternating delays)
	   Uniform
	   Gaussian
	   Gamma
	   Poison
	   Custom

Impairment Distributions	Drop, duplication and corruption probability is configurable up to 100%. Step size: 0.0001% Impairments (Duplication, Drop, Corruption) can be applied with very flexible distributions including Random, Periodic, Gilbert-Elliot, Gaussian, Gamma and Uniform. User can also specify custom distributions to be used with impairments.
Bandwidth Control (L1 / L2)	Policing - Step size: 100 kbps Shaping - Step size: 100 kbps

HARDWARE SPECIFICATIONS	
Oscillator characteristics	• Initial Accuracy is 3 ppm • Frequency drift over 1st year: +/- 3 ppm (over 15 years: +/- 15 ppm) • Temperature Stability: +/- 20 ppm (Total Stability is +/- 35 ppm)
Environmental	• Power; 60W • Operating Temperature: 10 to 30º C • Storage Temperature: -40 to 70°C • Humidity: 8% to 90% non-condensing
Regulatory	• FCC (US), CE (Europe)

How Chimera processes incoming traffic:
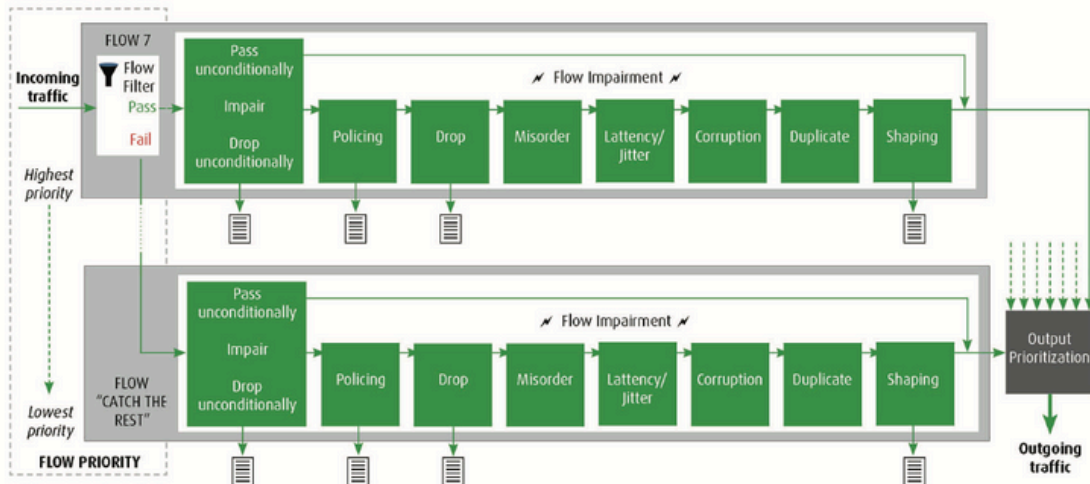
One module - multiple options

E100 Chimera 2 transceiver cages. The type of transceiver used determines the speed and number of ports available.
The port number / speed configuration must be the same for both cages and this is defined using XenaManager.

QSFP28/QSFP+
transceiver cage #1

2 x QSFP28 transceivers
Each transceiver:
- 1 x 100GE
- 2 x 50GE
- 1 x 40GE*
- 4 x 25GE
- 4 x 10GE*

Or

2 x QSFP+ transceivers
Each transceiver:
- 1 x 40GE
- 4 x 10GE

* Depending on transceiver capabilities

QSFP28/QSFP+
transceiver cage #2

Ordering Information

Product Description

- E100q Chimera 100GE 5-speed, 2 port impairment test module QSFP28
- E100qc Chimera 100GE 5-speed, 2 port impairment test module QSFP28 in a compact 1U chassis

Product Code

Chi-100G-5S-2P
C-Chi-100G-5S-2P