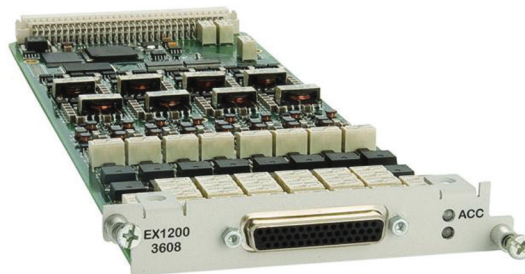


EX1200-3604 EX1200-3608

4-CHANNEL DAC/500 kSa/s AWG

8-CHANNEL DAC/500 kSa/s AWG



FEATURES

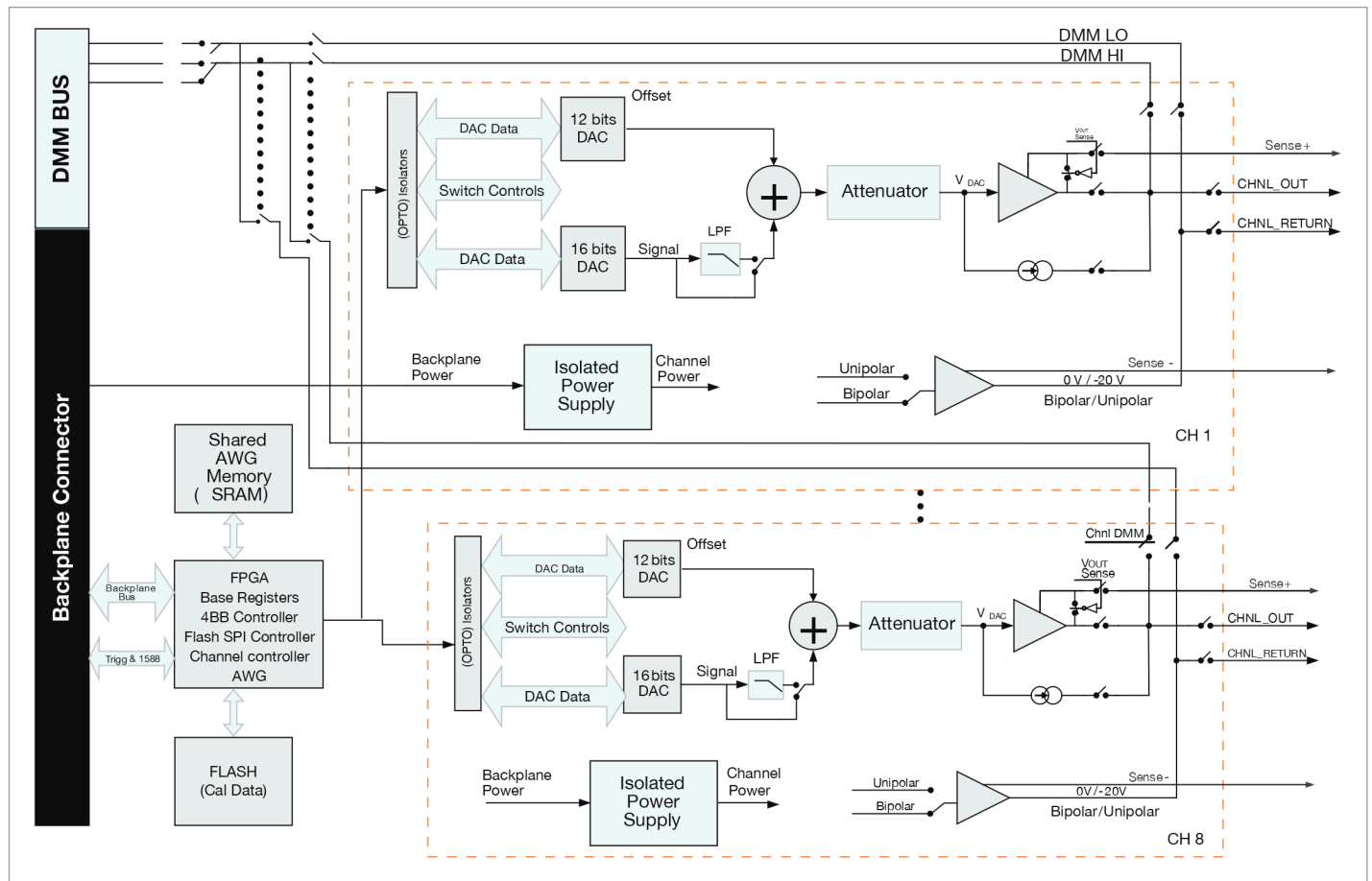
- 4 or 8 independent, isolated 16-bit D/A converters per instrument
- Ideal for simulating sensor outputs
- $\pm 20\text{V}$, $\pm 10\text{V}$, $\pm 5\text{V}$, $\pm 2\text{V}$ and $\pm 1\text{V}$ output ranges
- $\pm 20\text{ mA}$, $\pm 10\text{ mA}$, $\pm 5\text{ mA}$ output ranges
- Isolated outputs can be combined in series to extend range to 160 V or in parallel to achieve 160 mA
- 500 kSa/s arbitrary waveform generation with internal programmable clock
- Extensive triggering capability
- Synchronize level changes with input measurements to facilitate test sequencing
- Sense lines for every channel to compensate for cable loss and ensure highly accurate output

OVERVIEW

The EX1200-3608 and EX1200-3604 provide eight or four independent channels, respectively, of a digital to analog converter (DAC) with 16 bits of resolution. Each channel consists of a 16-bit DAC combined with a low-pass filter and an output amplifier. The 16-bit DAC allows these modules to achieve fine resolution at very low output range settings. Along with static output operation, the DAC modules provide an arbitrary waveform generation (AWG) mode which supports looping to build complex waveforms without the system controller’s intervention. The data may be paced out of the instrument by using either a user-supplied clock or the internal programmable timer with output rates up to 500 kSa/s.

Each channel is true-differential and has sense lines that can be used to compensate for voltage drops that occur over the length of the lead wire between the DAC output and the device under test (DUT). All channel outputs on these modules are individually isolated from system ground. This provides the ability to connect channels together in series to create an output channel with an extended range of 160 V or in parallel to create an output channel with a range of 160 mA.

An external clock input and an external trigger input are available to synchronize output level changes with external events. When used in an EX1200 series mainframe with the optional DMM, the DAC outputs can be routed to the internal analog backplane for verification prior to critical test runs to ensure the device will perform to a high degree of accuracy.



EX1200-3608 BLOCK DIAGRAM

General Specifications

Number of Channels	
EX1200-3604	4
EX1200-3608	8
Resolution	
16 bits, 16 bits monotonic	
Time/Frequency Domain	
Setting Time	5 μ s to 0.1% of specified value
Rise Time ¹	3 μ s typical
Slew Rate	40 V/ μ s typical
Bandwidth	250 kHz
Crosstalk ²	< 65 dBV @ 10 kHz
- Internal Channels	< 50 ns when all channels are running synchronized on the internal clock
- External Channels	< 100 ns when all channels are running synchronized on the internal clock
Time From Internal Trigger Receipt to First Sample Output	
2.2 μ s Plus the Rise Time	
External Clock	
Frequency	Maximum 500 kHz
Levels	LVTTL
External Trigger Input	
Pulse Width	Minimum 20 ns
Levels	LVTTL
Marker Output	
Levels	LVTTL
Duration	20 ns \div 1.34 s in 20 ns increments

DAC Specifications, Voltage Mode

POWER CONSUMPTION

EX1200-3604	
3.3 V	0.3 A
5 V	1 A
24 V	0.8 A
EX1200-3608	
3.3 V	0.3 A
5 V	1 A
24 V	1 A

OUTPUT VOLTAGE RANGES

Bipolar	± 1 V, ± 2 V, ± 5 V, ± 10 V, ± 20 V
Unipolar	40 V
Auto-Ranging	Supported
Maximum Output (series Channels)	± 160 V
Maximum Output	DC to maximum sampling rate
Output Current	± 20 mA
Current Protection	Current limitation circuit kicks in above 50 mA
Short Circuit Time ³	Up to 20 minutes. No restart necessary after short circuit



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DAC Specifications, Voltage Mode

DCV Accuracy	
1 V	±(0.05% of setting ±1.3 mV)
2 V	±(0.05% of setting ±1.6 mV)
5 V	±(0.07% of setting ±3.5 mV)
10 V	±(0.07% of setting ±4.0 mV)
20 V	±(0.06% of setting ±4.0 mV)
40 V	±(0.10% of setting ±8.0 mV)
DCV Noise	
	≤ 2 mV rms
Programmable Offset Range	
	full-scale
Ripple Noise, DCV	
	≤ 2 mV rms
Isolation Between Channels	
	200 V
Voltage Remote Sensing ⁴	
	High and low sense lines available per channel for cable length voltage drop compensation

DAC Specifications, Current Mode

Output Current Ranges	
Ranges	±5 mA, ±10 mA, ±20 mA
Maximum Output	±160 mA
- (Parallel Channels)	DC to 1 kHz sampling rate
- Maximum Frequency	DC to maximum sampling rate
Output Current Short Circuit	
Per Channel	±5 mA, ±10 mA, ±20 mA
Short Circuit Time ⁵	Up to 20 minutes. No restart necessary after short circuit.
DCA Accuracy	
1 kΩ Load	±(0.10% of setting +0.1% of range)
Other Load	Add + (3PPM/Ω * ABS(1kΩ-RL)) of setting
Compliance Voltage	
	20 V

AWG Specifications

Update Rate	
Programmable	20 ns (steps)
Maximum	500 kSa/s (2 μs) programmable, maximum 500 kSa/s
Output Current Short Circuit	
Per Channel	±5 mA, ±10 mA, ±20 mA
Short Circuit Time ⁵	Up to 20 minutes. No restart necessary after short circuit.
Trigger Sources	
	Front panel input, LXISync, software
Waveform Size	
Minimum	4 samples
Maximum	2,097,100 samples
Waveforms	
	1 to 4096 (SW limited can be increased in the future)
Sequences	
	1 to 4096 (SW limited can be increased in the future)
Waveform Repeat Count	
	1 to 2 ¹⁶ (65,536)
Memory Sequence Repeat (Burst) Count	
	1 to 2 ¹⁶ (65,536)
Steps per Sequence	
	1 to 4096 (SW limited can be increased in the future)
Modes	
IVI-compliant	Output modes: standard waveform, arbitrary waveform, arbitrary sequence Operation modes: continuous, burst
VTi Instrument Specific	Operation modes: sequenced, single step



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AWG Specifications

Marker Function	
Output	Can be sourced from any of the channels
Position	Can be placed at anywhere inside a waveform
Marker Pulse Length	20 ns to 0.335 s
Marker Output	Front panel TTL compatible output
Standard Waveforms	≤ 2 mV rms
Supported Waveforms	Sine, ramp (up/down), triangle, and square
Initial Phase	Supported for all standard waveforms
Burst Mode	Supported for all standard waveforms
Duty Cycle	Adjustable for all standard waveforms
Channel Configuration	Each channel is programmed independently in standard or AWG modes
Connector Type	44-pin

Notes:

- ¹ Measured 10% - 90% on a ±20 V square wave with 1 kΩ load, filter turned Off.
- ² Measured on CH5 with channels 0 through 4 and 6 through 7 producing a ±20 V square wave at 10 kHz
- ³ Longer short circuit times can damage the card.
- ⁴ Maximum sense line impedance is 10 Ω in either sense.
- ⁵ Longer short circuit times can damage the card.

Ordering Information

Models	Configuration
EX1200-3604	4-channel DAC/500 kSa/s AWG
EX1200-3608	8-channel DAC/500 kSa/s AWG
Accessories and Tools	
70-0363-502	44-pin HD D-sub mating connector and backshell, with 3ft unterminated 22 AWG wire
70-0367-007	EX1200-TB44, 44p DIN connector with internal CJC reference
27-0390-044	44-pin HD D-sub mating connector, backshell and pins, crimp style
70-0297-001	Crimp tooling, includes handle and positioner, 22 AWG
70-0363-502	44-pin, unterminated cable assembly, 3 ft



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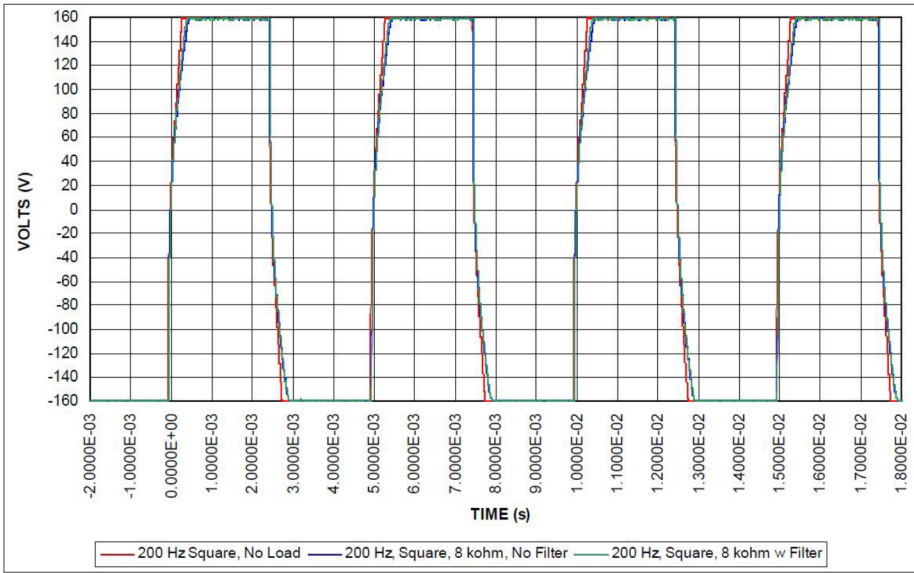


FIG. 1: CONNECTING CHANNELS IN SERIES

When wiring channels in series, all channels must have the same waveform. Each channel must also have the same filter setting to eliminate a possible slew rate conflict between the channels. The channels must also have similar amplitudes to ensure that the waveform will be equally distributed among the channels. The waveforms in the figure above shows an EX1200-3608 with all eight channels wired in series. Because each channel has some common mode capacitance relative to chassis, bandwidth will be limited. In the examples shown below, the waveform is set to 200 Hz. When fully loaded to 20 mA, a small reduction in the square wave slew rate can be seen in the blue trace.

WARNING: High-voltage waveforms can be potentially dangerous. Use extreme caution when wiring any EX1200-360x channels in series.

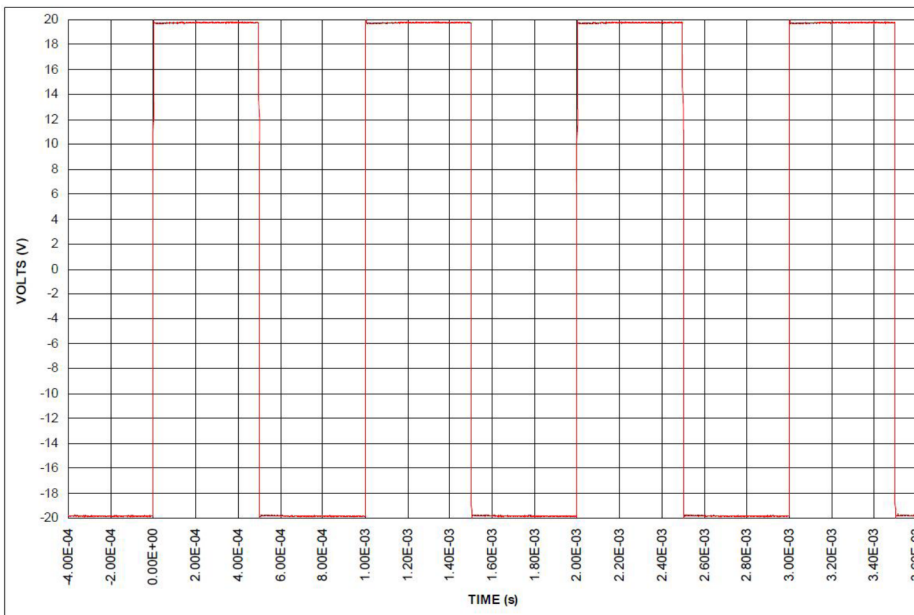


FIG. 2: CONNECTING CHANNELS IN PARALLEL

As is true when wiring voltage channels in series, channels wired in parallel wiring must 1) be set to output the same waveform, 2) be set to the same frequency, 3) be in the same phase, and 4) be set to the same filter setting. All of the parallel channels must have similar amplitudes to ensure that the waveform is equally distributed among the channels. Because each channel has the same small common mode capacitance, relative to chassis, the bandwidth will be much higher than for voltage mode.



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