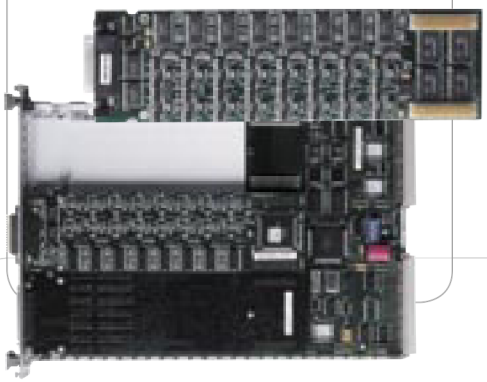
VM3608A 8-channel, 16-bit DAC/AWG (VMIP™)

VM3616A 16-channel, 16-bit DAC/AWG (VMIP™)



Overview

The VM3616A provides 16 independent channels of a digital to analog converter (DAC) with 16 bits of resolution. Each channel consists of an independent DAC combined with an output amplifier. Along with static output operation, the VM3616A provides a FIFO mode where the selected channels can accept and output a continuous stream of data. The VM3616A also offers arbitrary waveform generation (AWG) mode which supports sophisticated looping and branching to build complex waveforms without the system controller's intervention. The data may be paced out of the instrument by using either a user-supplied clock or the internal programmable timer.

The VM3616A is the highest density arbitrary waveform generator available on the VXIbus platform, offering up to 48 channels in a single-wide, C-size VXIbus module, and is ideal for automotive and medical applications where multiple low frequency signals need to be generated.

This module is part of the VMIP™ family of instruments and can be combined with up to two other modules to form a high-density VXIbus instrument that fully utilizes the capabilities of the VMIP™.

Programming

All of the module's settings are programmed via the VXIbus word serial interface. The commands are both IEEE-488.2 and SCPI compatible. Additionally, the DAC output values may be programmed using direct register access providing maximum speed. In FIFO mode, the data stream is sent to the instrument via direct register access. In arbitrary waveform generator mode, the waveform data may be input using either word serial data access or register-based data access.

For programming ease, VXI*plug&play* drivers are provided.

Data Setup and Scan Lists

Normal Mode - In normal mode, all channels are set to static values via word serial commands or through direct register access. To support higher throughput, 512 predefined values for each channel may be loaded into RAM. With a single word serial command, all 16 channels are updated at once. To facilitate synchronization, all channels are double buffered, and any channel may be programmed to update all outputs. This allows multiple values to be changed, but all channels will update at the same time. Updates can also be synchronized to the front panel trigger input, the VXIbus TTL trigger lines, or via a word serial command.

Features

- 16 Independent 16-bit D/A Converters per Instrument
- Up to 48 D/A Converters per VXIbus C-Size Slot
- ±20 V and ±10 V Output Ranges
- 100 kSa/s Arbitrary Waveform Generation with Internal Programmable Clock
- FIFO Mode Allows High-speed Uninterrupted Data Output
- Extensive Triggering Capability
- SCPI Compatible
- VXIplug&play Drivers

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FIFO Mode - In FIFO mode, any or all channels may be set up to output a continuous stream of data, while all other channels remain at their previously programmed values. Data is fed into the instrument using direct register access and data throughput of up to 100 kSa/s. The output may be paced using an internal timer with 100 nS resolution, the VXIbus TTL trigger lines or via a front panel trigger input.

Arbitrary Waveform Generator Mode - In arbitrary waveform generator mode, any or all channels may be set up to output complex waveforms by loading one or more waveform segments and linking them together. All other channels remain at their previously programmed values. Up to 4096 waveform segments may be loaded into the instrument and 4096 segments may be linked together. Each segment may be used once, looped up to a million plus times, or may loop continuously until triggered to advance to the next segment. Advancing from segment to segment can occur automatically, or when a trigger event is received. In arbitrary waveform generator mode, all enabled channels are synchronized with each other, and all waveform segments for each channel are the same length. All looping and branching instructions apply for all enabled channels.

Scan Mode - In scan mode, any or all channels may be set up to output data previously stored in RAM. Each channel may have up to 512 data points, and each channel may have a unique number of points. The data is advanced by a VXIbus TTL trigger event or the front panel trigger input. Scan mode may be set up to either stop at the end of the data set, or restart from the beginning of the data set. In this mode, the output levels of the channels that are not included in scan mode may be altered while scan mode is running.

Calibration

The calibration constants are stored in non-volatile memory, are determined when the instrument is calibrated, and can be changed as necessary (such as during routine calibration cycles or when the user selects a new gain setting and wishes to set the gain accurately). These constants may also be queried at any time and altered as necessary if the security code is known. All calibration is done using calibration DACs to adjust the gain and offset of each channel, eliminating the need to remove the covers from the unit while calibrating. The accuracy of the instrument is maintained when direct register access is used.

Specifications

Output Ranges:	±20 V, 610 µV step, or ±10 V, 305 µV step
Output Current:	±50 mA per channel (1 A max. total for all channels per C-size VXIbus card)
Resolution:	16 bits, 16 bits monotonic
Short Circuit:	Continuous duration
Slew Rate:	6 V/µs (50 mA load)
Settling time:	10 µs to 0.1% of specified value
Gain Error:	±0.015% + 0.002%/°C
Offset Error:	±2 LSB + 0.2 LSB/°C
Conversion Rate:	100,000 voltage changes per second, normal mode register access, FIFO mode, and AWG mode. 100 voltage changes per second, normal mode word serial access.
Static Mode Update Sources:	VXIbus TTL trigger bus 0-7 Front panel input Updating any selected channel word serial command
Memory:	512 kwords, 1 Mword optional
FIFO Memory:	512 kwords divided by the number of active channels 1 Mword optional
FIFO Clock Source:	Any trigger source
AWG Memory:	484 kwords divided by the number of active channels 996 kword optional
AWG Data Traces:	1 to 4096 unique patterns
AWG Segments:	1 to 4096
AWG Loop Count:	1 to 1048575 or continuous

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AWG Advance Modes:	Synchronous: waits for the end of the current pattern to advance to the next. Asynchronous: advances immediately to the next pattern upon being triggered.
AWG Advance Conditions:	Automatic or triggered
AWG Marker Function:	Marks the first data in a pattern when enabled. Polarity is software programmable.
AWG Marker Output:	VXIbus TTL trigger bus 0-7 Front panel TTL compatible output.
Trigger Source:	VXIbus TTL trigger bus 0-7 Front panel input, TTL compatible Internal timer. Word serial command
Advance Clock Source:	VXIbus TTL trigger bus 0-7 Front panel input, TTL compatible Internal timer Word serial command

General

Instrument drivers:	The module is provided with VXI*plug&play* drivers
User Connector:	Standard 44-pin female high-density D-Sub connector. A mating male solder cup connector is provided with each unit

Ordering Information

VM3616A	16-channel 16-bit D/A
VM3608A	8-channel 16-bit D/A (must be configured with a VM9000 host module)
Option 4:	1 Megaword Memory